Document Title

128K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Date	Remark
0.0	-. Initial Draft	May 09 2003	Preliminary
0.1	-. Add Pb-free part number	Feb. 13 2004	
0.2	-. Add 45ns part specification	Mar. 20 2009	
	-. I_{SB1}(Typ.) changed from 0.5uA to 0.3uA		
	-. I_{SB1}(Max.) changed from 5uA to 1.5uA		
	-. t_{CW1}, t_{CW2}, t_{AW} changed from 45ns to 40ns with 55ns part		
	-. t_{WP} changed from 40ns to 30ns with 55ns part		
	-. t_{WP} changed from 50ns to 35ns with 70ns part		
	-. Memory Function Guide updated in the last page		
1.0	-. EM610FV8(KGD), EM610FV8S series, EM610FV8T series & EM610FV8V series are unified to EM610FV8 Family	Apr. 07 2009	Release
	-. t_{WHZ} changed from 20ns to 25ns with 70ns part		
	-. t_{CW1}, t_{CW2}, t_{AW} changed from 40ns to 35ns with 45ns part		
1.1	-. Change function description when CS pin is 'L' status	Nov 21 2012	
1.2	-. Change 8x13 sTSOP package information	Dec 18 2012	
2.0	-. Change company name & logo	Mar 29 2013	

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FEATURES

- Process Technology : 0.18μm Full CMOS
- Organization : 128K x 8 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V (Min)
- Three state output and TTL Compatible
- Package Type
  - 32-sTSOP1, 32-TSOP1, 32-SOP

GENERAL DESCRIPTION

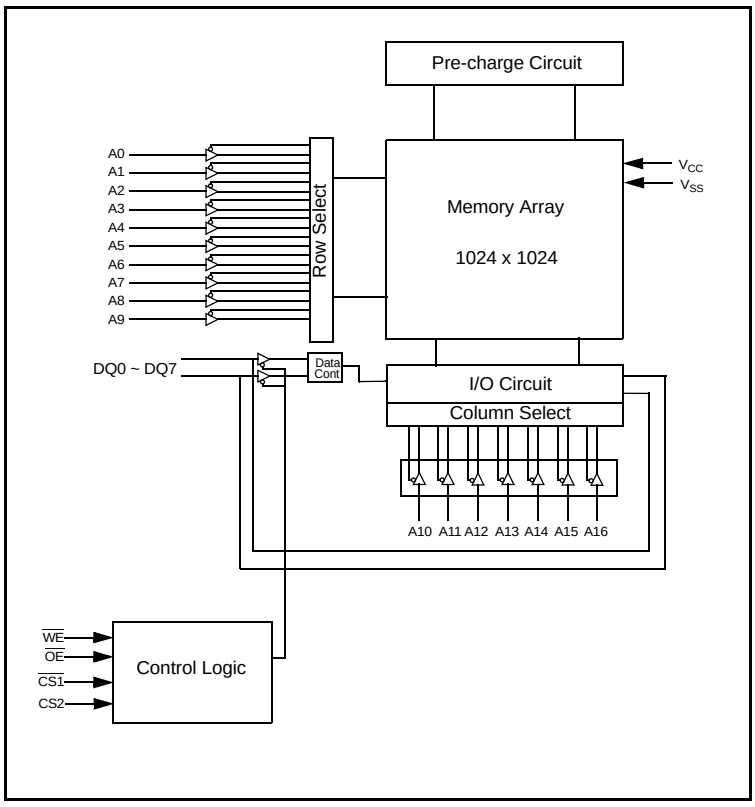
The EM610FV8 families are fabricated by JSC's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Typ.)	Operating (I_{CC1}.Max.)	
EM610FV8	Industrial (-40 ~ 85°C)	2.7 ~ 3.6 V	45/55/70 ns	0.3 μA[2]	3 mA	KGD
EM610FV8S - xx[1]LF						32-sTSOP1
EM610FV8T - xx[1]LF						32-TSOP1
EM610FV8V - xx[1]LF						32-SOP

1. "xx" represents speed.
2. Typical values are measured at V_{CC}=3.3V, T_A=25°C and not 100% tested.

FUNCTIONAL BLOCK DIAGRAM



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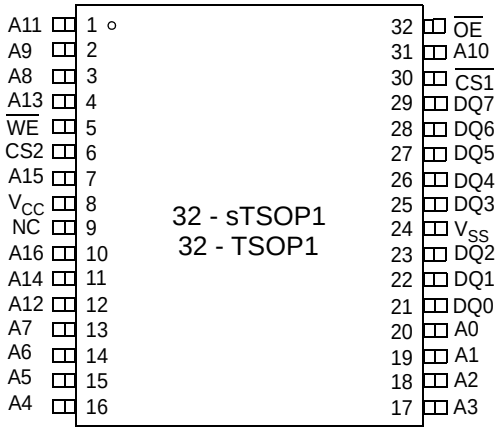
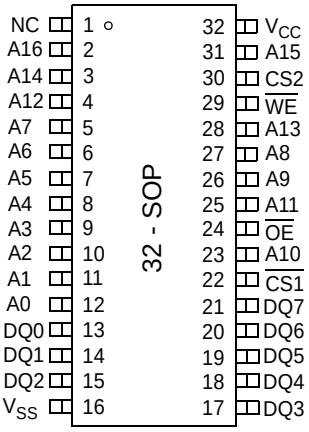
PIN CONFIGURATIONS

32 - sTSOP1, 32 - TSOP1 : Top view



32 - SOP : Top view



PIN DESCRIPTION

Name	Function	Name	Function
$\overline{CS}_1$, CS_2	Chip Select input	V_{CC}	Power Supply
$\overline{OE}$	Output Enable input	V_{SS}	Ground
$\overline{WE}$	Write Enable input		
A0~A16	Address inputs		
DQ0~DQ7	Data inputs/outputs		

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ABSOLUTE MAXIMUM RATINGS[1)]

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.2 to 4.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	^oC

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	DQ0~7	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

NOTE : X means don't care. (Must be low or high state)

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RECOMMENDED DC OPERATING CONDITIONS [1)]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	V_{CC} + 0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. TA= -40 to 85°C, otherwise specified
2. Overshoot: VCC +2.0 V in case of pulse width ≤ 20ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Ouput capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} or V_{IO}=V_{SS} to V_{CC}		-1	-	1	μA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}		-	-	3	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, CS_2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V		-	-	3	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	45ns	-	-	30	mA
			55ns	-	-	25	
			70ns	-	-	20	
Output low voltage	V_{OL}	I_{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Standby Current (TTL)	I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}, Other inputs=V_{IH} or V_{IL}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS_1}$≥V_{CC}-0.2V, CS_2≥V_{CC}-0.2V ($\overline{CS_1}$ controlled) or 0V≤CS_2≤0.2V (CS_2 controlled), Other inputs = 0~V_{CC} (Typ. condition : V_{CC}=3.3V @ 25°C) (Max. condition : V_{CC}=3.6V @ 85°C)	LL LF	-	0.3[1)]	1.5	μA

1. Typical values are measured at V_{CC}=3.3V, T_A=25°C and not 100% tested.

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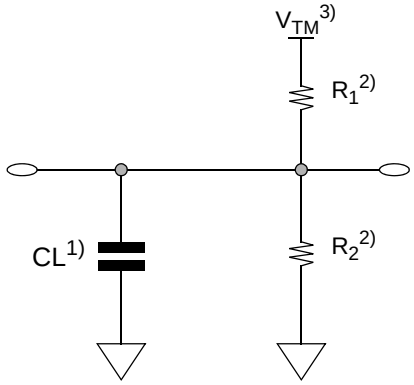
AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)
Input Pulse Level : 0.4 to 2.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : $CL^{1)}$ = 100pF+ 1 TTL (70ns)
$CL^{1)}$ = 30pF + 1 TTL (45ns/55ns)



1. Including scope and Jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM} = 2.8V
4. CL = 5pF + 1 TTL (measurement with tLZ, tOLZ, tHZ, tOHZ, tWHZ)

READ CYCLE (V_{cc} = 2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	45	-	55	-	70	-	ns
Address access time	t_{AA}	-	45	-	55	-	70	ns
Chip select to output	t_{CO1}, t_{CO2}	-	45	-	55	-	70	ns
Output enable to valid output	t_{OE}	-	25	-	25	-	35	ns
Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	10	-	10	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	20	0	20	0	25	ns
Output disable to high-Z output	t_{OHZ}	0	20	0	20	0	25	ns
Output hold from address change	t_{OH}	10	-	10	-	10	-	ns

WRITE CYCLE (V_{cc} = 2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	45	-	55	-	70	-	ns
Chip select to end of write	t_{CW1}, t_{CW2}	35	-	40	-	60	-	ns
Address setup time	t_{AS}	0	-	0	-	0	-	ns
Address valid to end of write	t_{AW}	35	-	40	-	60	-	ns
Write pulse width	t_{WP}	30	-	30	-	35	-	ns
Write recovery time	t_{WR}	0	-	0	-	0	-	ns
Write to ouput high-Z	t_{WHZ}	0	20	0	20	0	25	ns
Data to write time overlap	t_{DW}	25		25		30		ns
Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
End write to output low-Z	t_{OW}	5	-	5	-	5	-	ns

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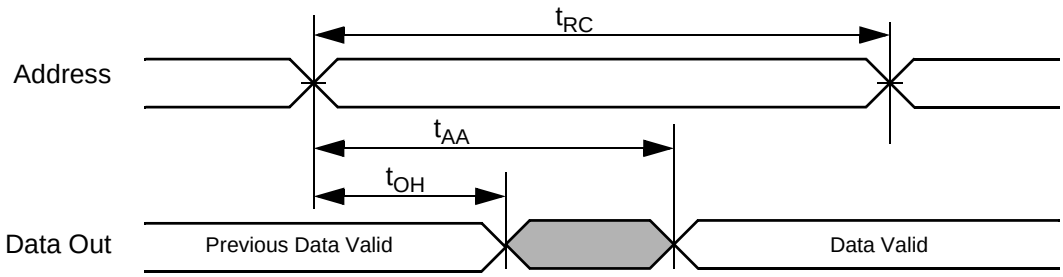
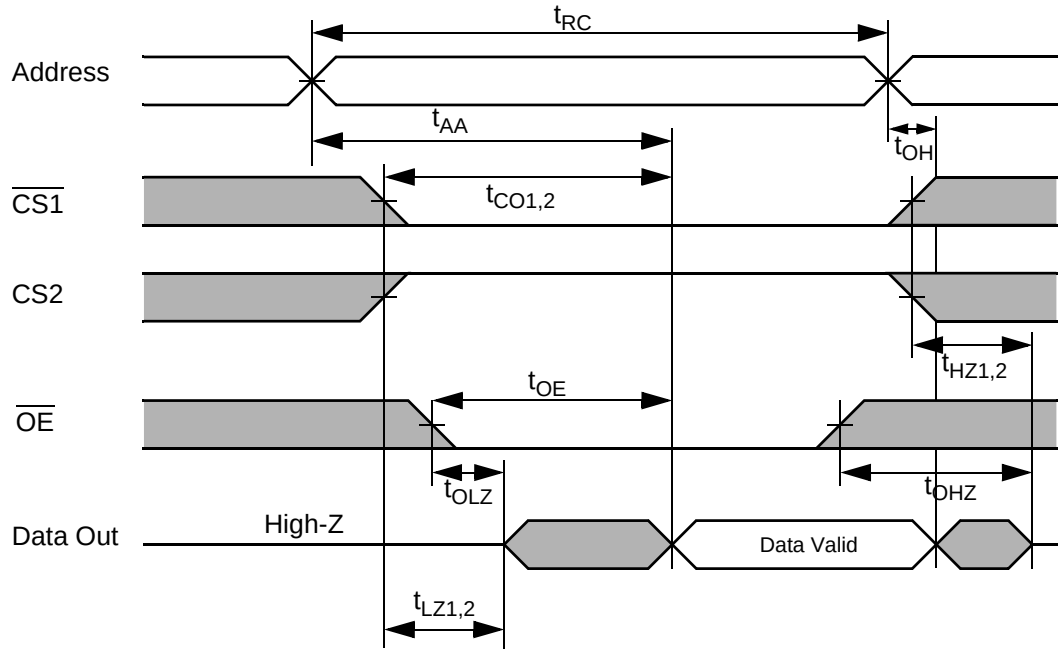
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH})



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



NOTES (READ CYCLE)

1. $t_{HZ1,2}$ and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ1,2}$(Max.) is less than $t_{LZ1,2}$(Min.) both for a given device and from device to device interconnection.

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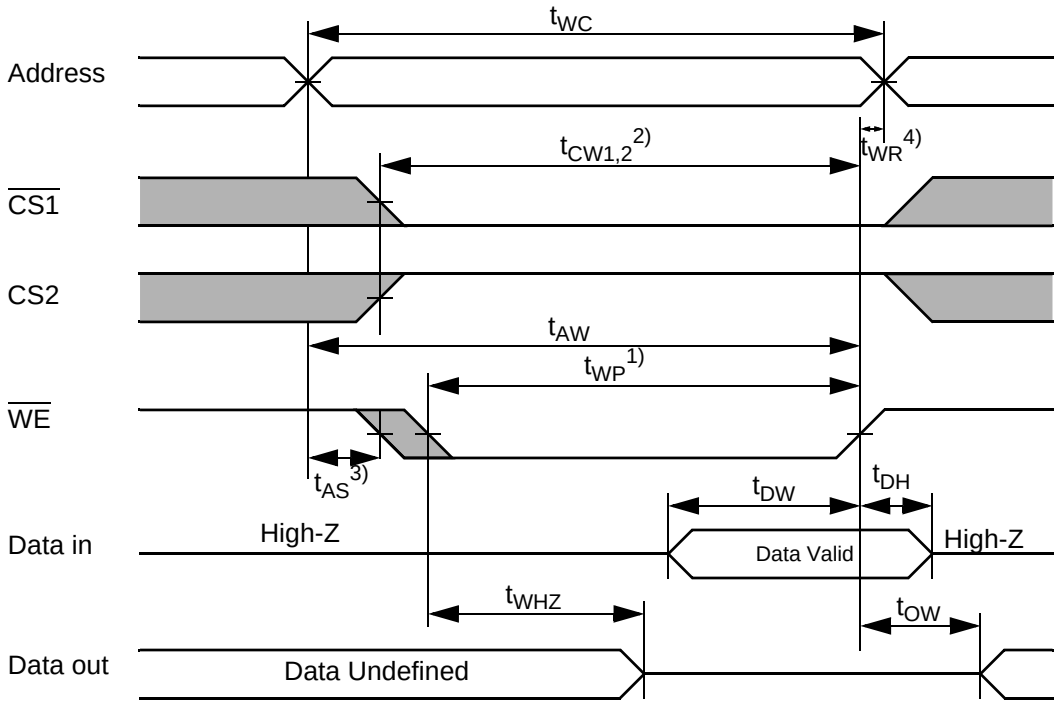
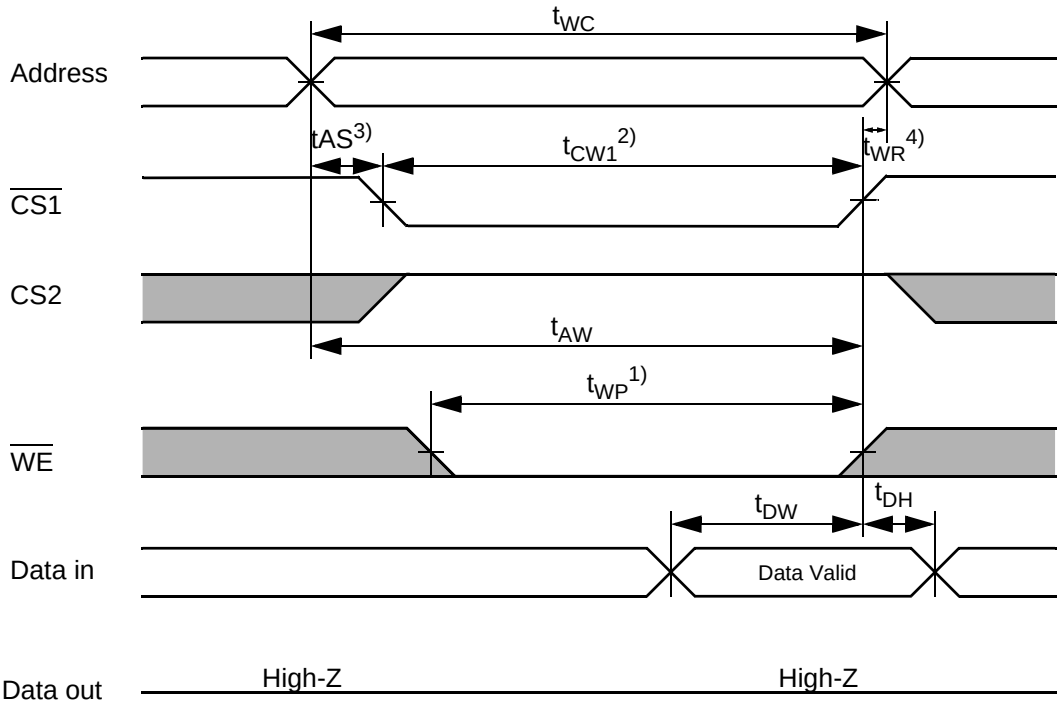
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



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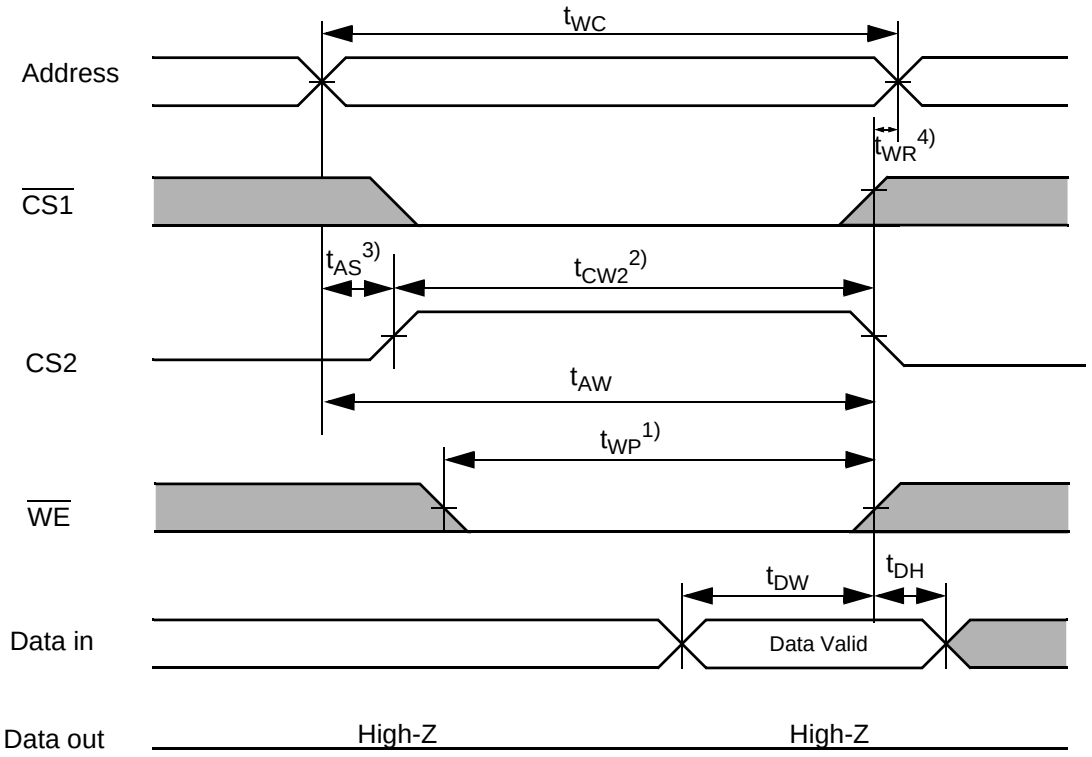
TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the lastest transition among $\overline{CS1}$ goes low, CS2 goes high and $\overline{WE}$ goes low. A write ends at the earliest transition when $\overline{CS1}$ goes high, CS2 goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high.

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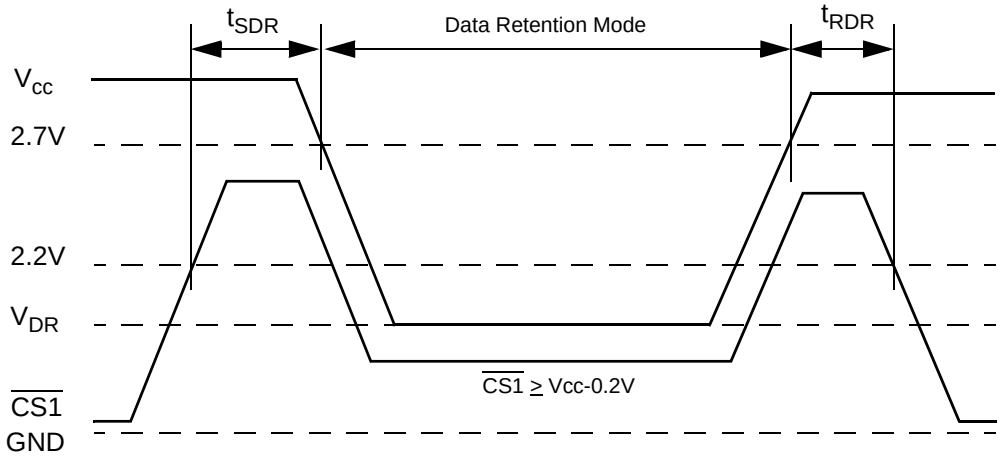
DATA RETENTION CHARACTERISTICS

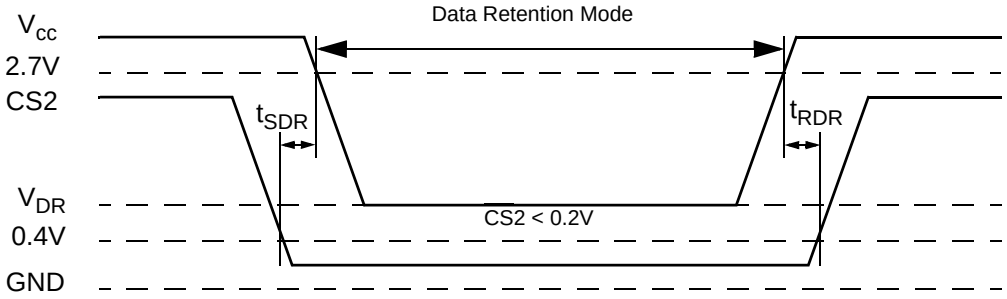
Parameter	Symbol	Test Condition	Min	Typ[2)]	Max	Unit
V_{CC} for Data Retention	V_{DR}	I_{SB1} Test Condition (Chip Disabled) [1)]	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC}=1.5V, I_{SB1} Test Condition (Chip Disabled) [1)]	-	0.25	-	μA
Chip Deselect to Data Retention Time	t_{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t_{RDR}		t_{RC}	-	-	

NOTES

1. See the I_{SB1} measurement condition of datasheet page 5.
2. Typical values are measured at T_A=25°C and not 100% tested.

DATA RETENTION WAVE FORM





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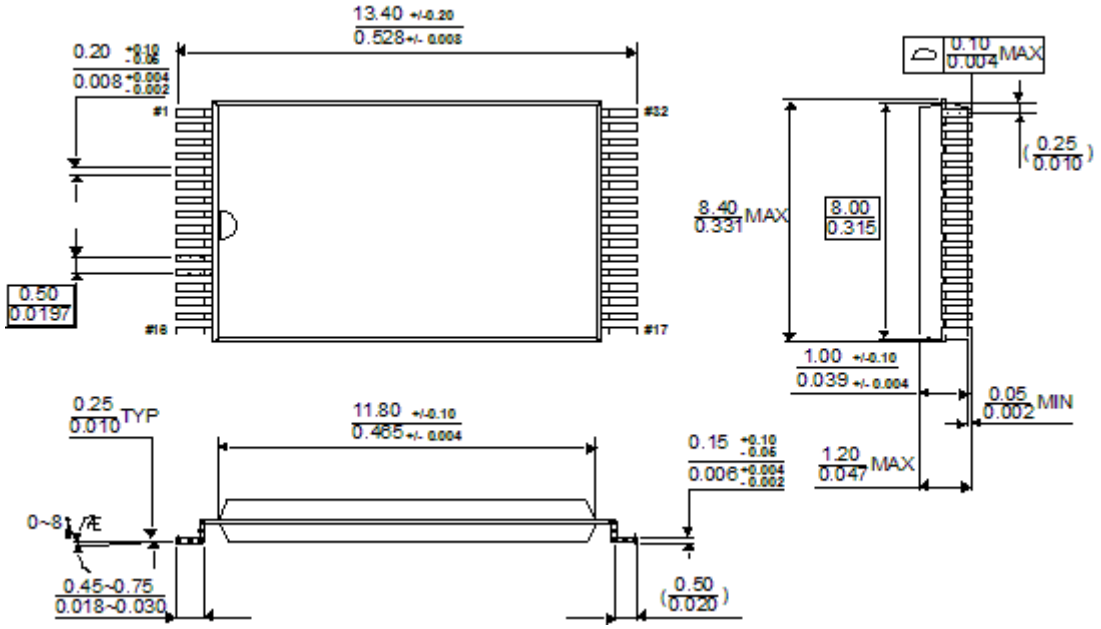
PACKAGE DIMENSIONS

32Pin - sTSOP Type1

Unit : millimeters/Inches



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32Pin - TSOP Type1

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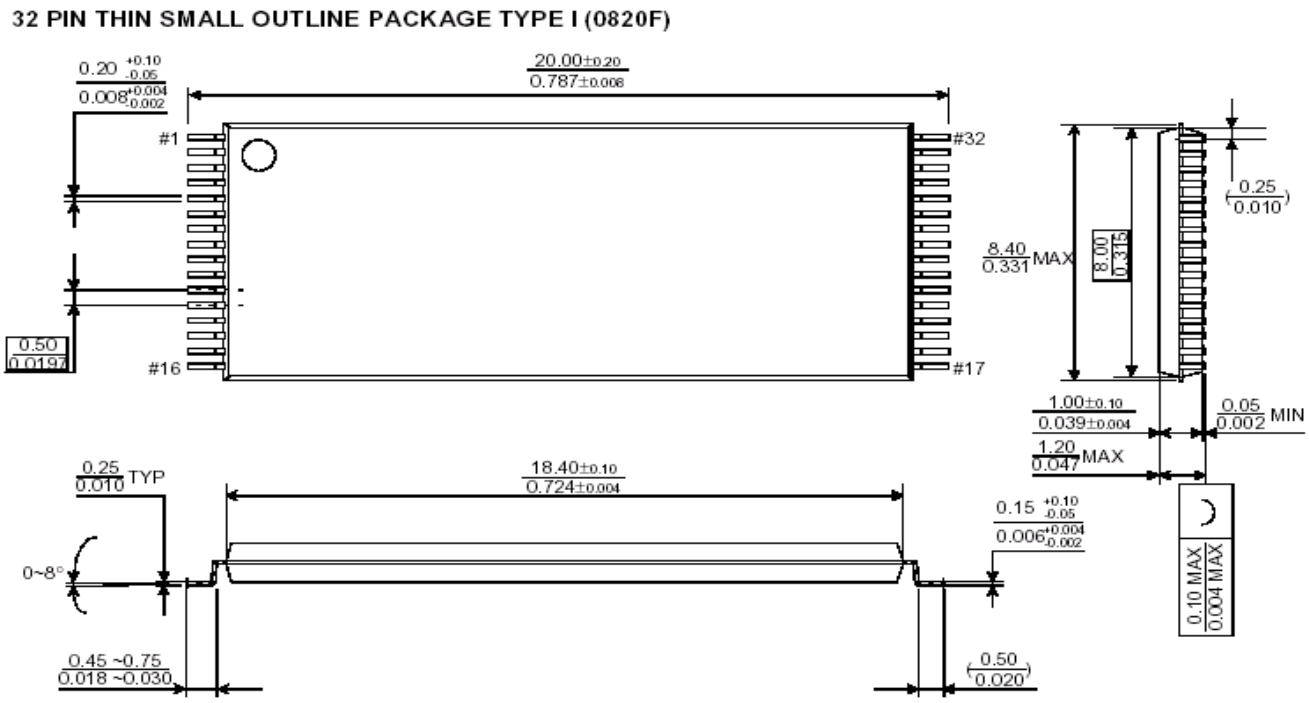

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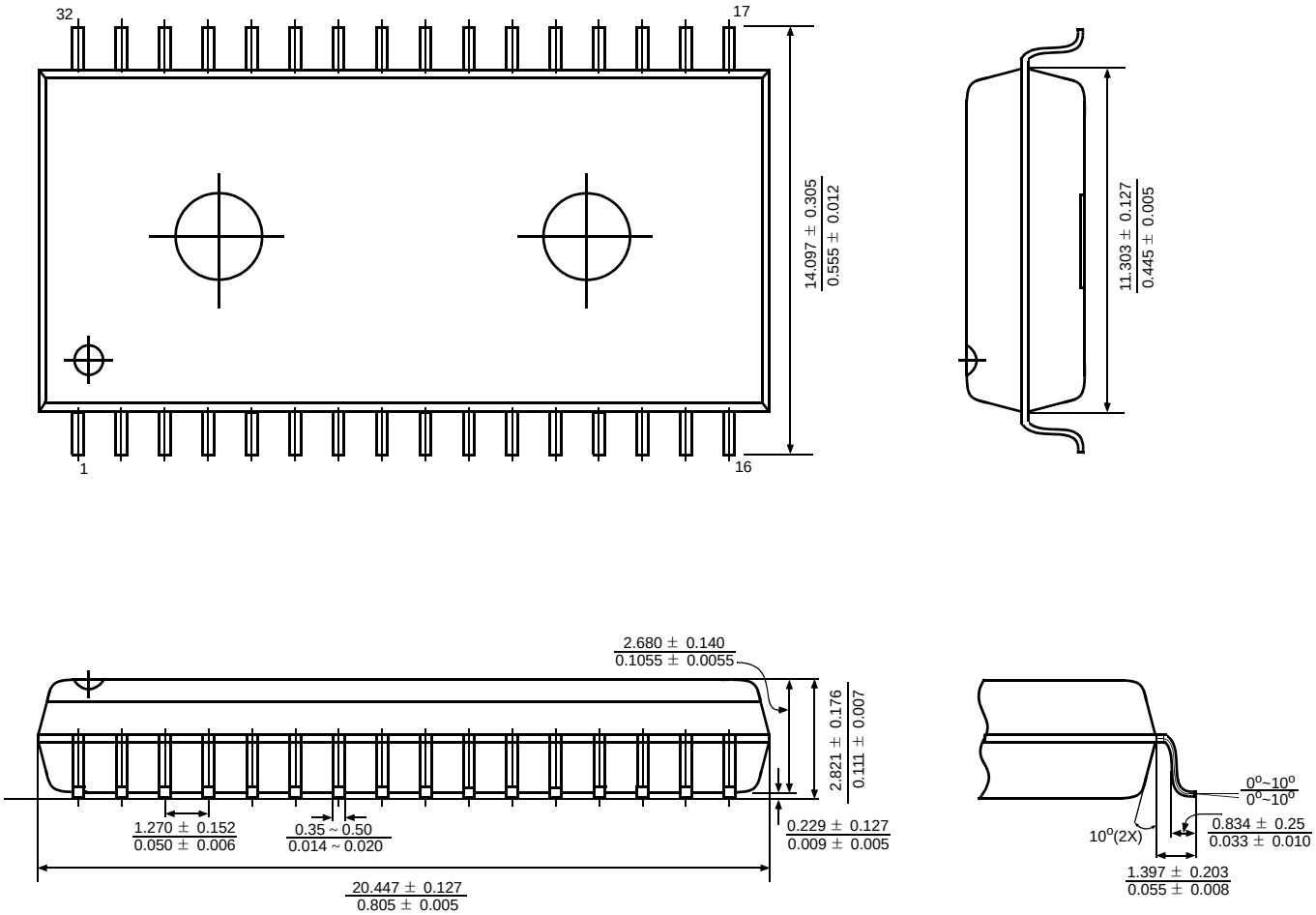
PACKAGE DIMENSIONS

32Pin - SOP

Unit : millimeters/Inches



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MEMORY FUNCTION GUIDE

EM X XX X X X XX X X - XX XX

1. JSC Memory
2. Device Type
3. Density
4. Function
5. Technology
6. Operating Voltage
7. Organization
8. Version
9. Package
10. Speed
11. Power

1. Memory Component

2. Device Type

6	----------	Low Power SRAM
7	----------	STRAM
C	----------	CellularRAM

3. Density

1	----------	1M
2	----------	2M
4	----------	4M
8	----------	8M
16	----------	16M
32	----------	32M
64	----------	64M
28	----------	128M

4. Option

0	----------	Dual CS
1	----------	Single CS

5. Technology

F	----------	Full CMOS

6. Operating Voltage

T	----------	5.0V
V	----------	3.3V
U	----------	3.0V
S	----------	2.5V
R	----------	2.0V
P	----------	1.8V

7. Organization

8	----------	X8 bit
16	----------	X16 bit
32	----------	X32 bit

8. Version

Blank	----------	Mother die
A	----------	2 nd generation
B	----------	3 rd generation
C	----------	4 th generation
D	----------	5 th generation
E	----------	6 th generation
F	----------	7 th generation
G	----------	8 th generation

9. Package

Blank	----------	KGD, FBGA
S	----------	32 sTSOP1
T	----------	32 TSOP1
U	----------	44 TSOP2
V	----------	32 SOP

10. Speed

45	----------	45ns
55	----------	55ns
60	----------	60ns
70	----------	70ns
85	----------	85ns
90	----------	90ns
10	----------	100ns
12	----------	120ns

11. Power

LL	----------	Low Low Power
LF	----------	Low Low Power(Pb-free & Green)
L	----------	Low Power
S	----------	Standard Power

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