HTT035A01

产品名称（**Product name**）：单色 TFT 模组

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1. Basic Specifications

1.1 Display Specifications

1>LCD Display Mode	Mono-TFT , Normal Black VA
2>Viewing Angle	Wide View
3>Driving Method	TFT Active Matrix
4>Interface	8080/6800/4L/3L Interface
5>Backlight:	8 Pcs White LED (Parallel)
6>Controller/Driver	TBD/ST7511

1.2Mechanical Specifications

1>Outline Dimension	58.56(L)x79.94 (W)x1.6(H)mm(Detailed Information refer to LCM Drawing)
2>Active Area	53.28(L)x71.04(W)
3>Pixel Pitch	0.222(L)x0.222(W)

2. Absolute Maximum Ratings

Items	Symbol	Condition	Unit
I/O Power Supply Voltage	VDDI	-0.3 ~ 6.0	V
Analog Power Supply Voltage	VDDA	-0.3 ~ 6.5	V
Analog Power Supply Voltage	VDDP	-0.3 ~ 6.0	V
LCD Power Supply Voltage	AVDD, GVDD	7.0	V
	AVCL, GVCL, VCOM	-7.0	V
	VGH － VGL	25	V
MPU Interface Input Voltage	VIN	-0.3 ~ VDDI +0.3	V
Operating Temperature	TOP	-30~+85	° C
Storage Temperature	Tst	-40~+90	° C

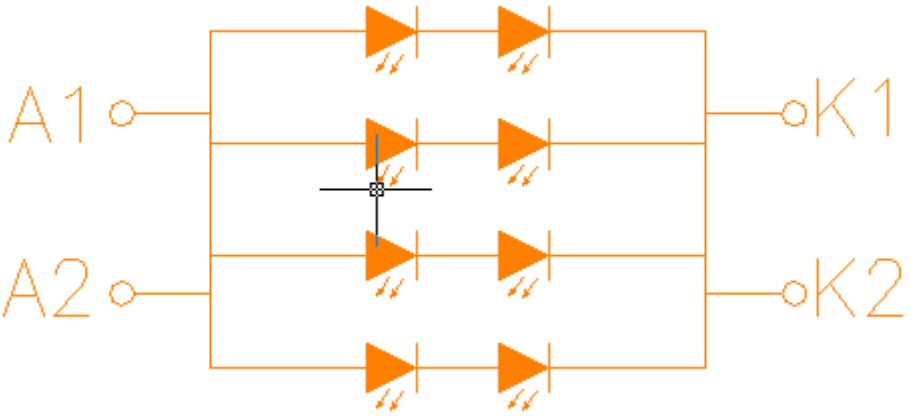
3. Electrical Characteristics

3.1 DC Characteristics

Items	Symbol	Rating			Unit	Condition	Applicable pin
		MIN.	TYP.	MAX.			
Operating Voltage	VDDI	2.7	-	5.5	V	External Supply	VDDI
Operating Voltage	VDDA	2.7	-	5.5	V	External Supply	VDDA
Operating Voltage	VDDP	2.7	-	5.5	V	External Supply	VDDP
Operating Voltage	VCCO	-	1.8	-	V	Built-in Power Supply	VCCO
Operating Voltage	AVDDO	6.1	-	9	V	Built-in Power Supply	AVDDO
Operating Voltage	AVCLO	-9	-	-6.1	V	Built-in Power Supply	AVCLO
Operating Voltage	GVDD	3.1	-	6.2	V	Built-in Power Supply	GVDD
Operating Voltage	GVCL	-6.2	-	-3.1	V	Built-in Power Supply	GVCL
Operating Voltage	VGH	8.0	-	19.0	V	Built-in Power Supply	VGH
Operating Voltage	VGL	-15.0	-	-5.0	V	Built-in Power Supply	VGL
Operating Voltage	VCOM	-2.0	-	-0.425	V	Built-in Power Supply	VCOM
Input High -Level Voltage	VIH	0.8VDDI	-	VDDI	V		MPU Interface
Input High -Level Voltage	VIL	VSS	-	0.2VDDI	V		MPU Interface
Output High -Level Voltage	VOH	0.8VDDI	-	VDDI	V	VDDI=2.7V,IOL=1mA	D[7:0]
Output Low -Level Voltage	VOL	VSS	-	0.2VDDI	V	VDDI=2.7V,IOL=1mA	D[7:0]
Input Leakage Current	ILI	-1.0	-	1.0	μA	VIN=VDDI or DGND	MPU Interface

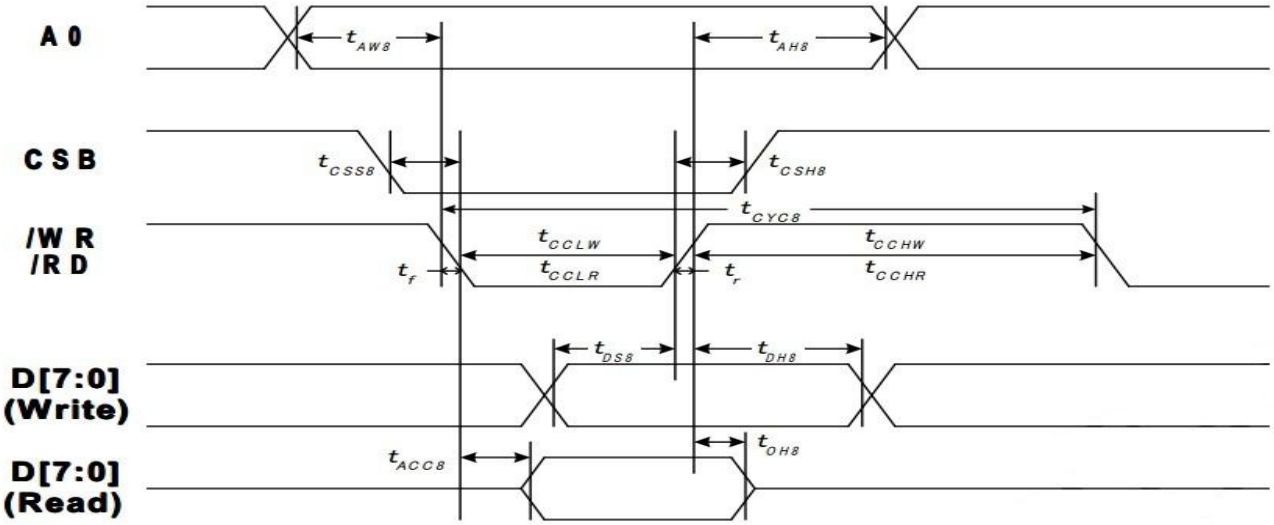
3.2 LED Backlight Circuit

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Average Brightness (without LCD)	IV	TBD	3000	-	cd/m^2	IF=15mA*8
Operating Temperature	Top	-30	-	80	℃	-
Storage Temperature	Tst	-40	-	80	℃	-
Solder Temp. For 3 Seconds	-	-	-	260	℃	-
Power consumption	White	-	60	-	mA	Ta=25℃ BLV =6.1V



3.3 AC Characteristics

3.3.1 System Bus Timing for 8080 Series MPU



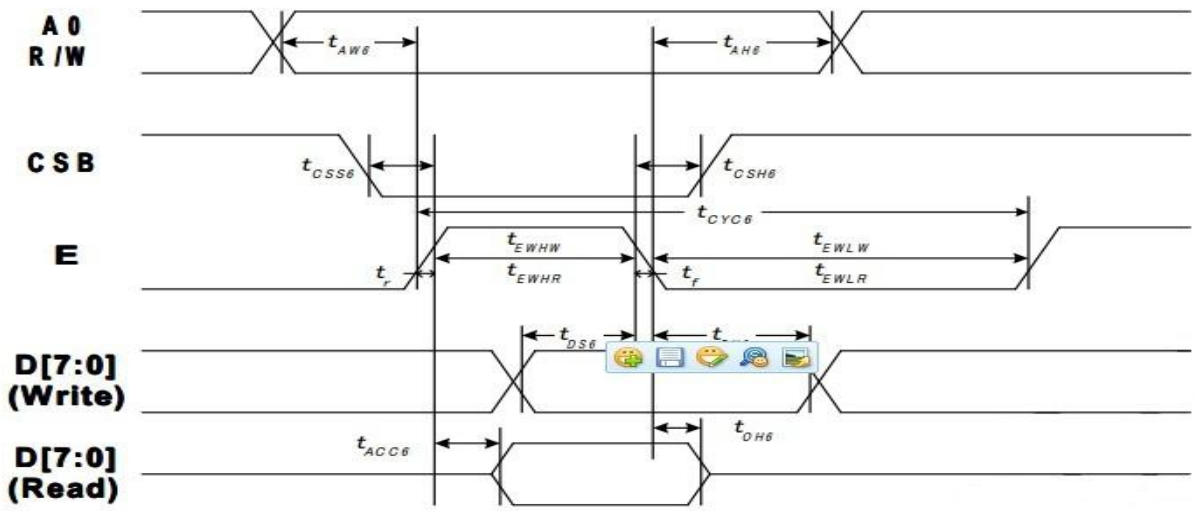
AGND=PGND=DGND=0V,VDDA=VDDP=VDDI=3.0~5.0V,Ta=25° C

Item	SIgnal	Symbol	Condition	Min	Max	Unit
Address setup time	AO	tAW8		10	-	ns
Address hold time		TAH8		0	-	
System cycle time	/WR	TCYC8		1100	-	
/WR L pulse width(WRITE)		TCCLW		500	-	
/WR H pulse width(WRITE)		TCCHW		500	-	
/RD L pulse width(READ)	/RD	TCCLR		950	-	
/RD H pulse width(READ)		TCCHR		500	-	
CSB setup time	CSB	TCSS8		100	-	
CSB hold time		TCSH8		100	-	
WRITE Data setup time	D[7:0]	TDS8		200	-	
WRITE Data hold time		TDH8		50	-	
READ access time		TACC8	CL=100pF	-	950	
READ Output disable time		TOH8	CL=100pF	5	200	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDDI as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level.CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns widther than /WR (or /RD).

3.3.2 System Bus Timing for 6800 Series MPU



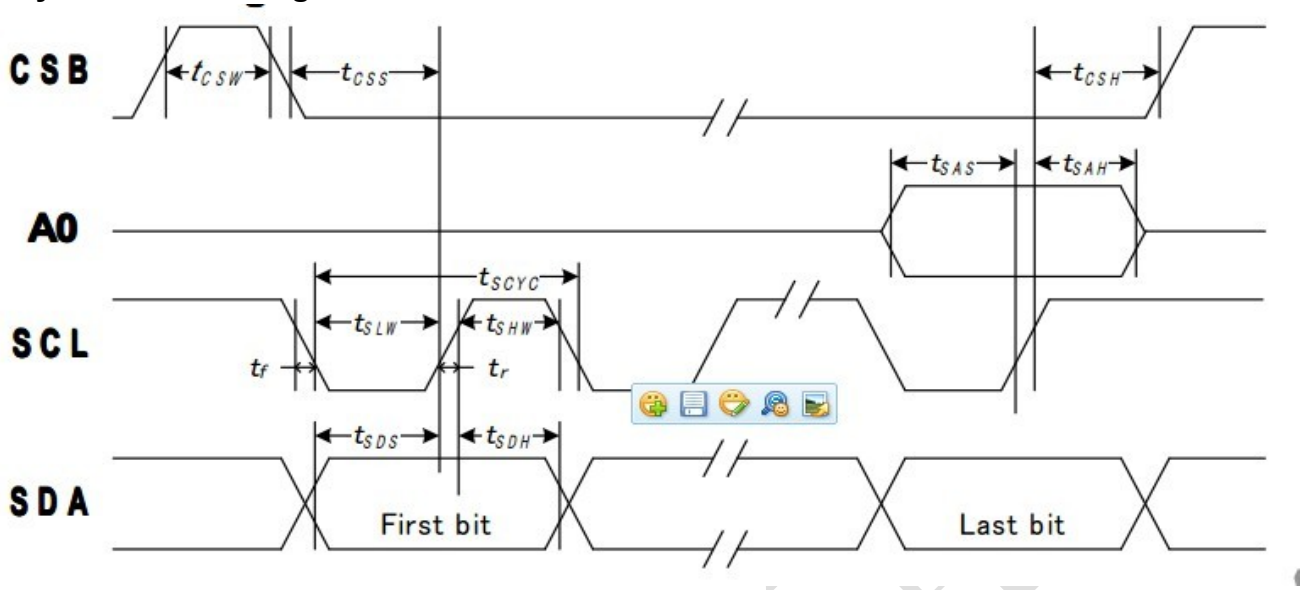
AGND=PGND=DGND=0V,VDDA=VDDP=VDDI=3.0~5.0V,Ta=25° C

Item	SIgnal	Symbol	Condition	Min	Max	Unit
Address setup time	AO	TAH6		10	-	ns
Address hold time		TAH6		0	-	
System cycle time	E	TCYC6		1100	-	
Enable L pulse width(WRITE)		TEWLW		500	-	
Enable H pulse width(WRITE)		TEWHW		500	-	
Enable L pulse width(READ)		TEWLR		500	-	
Enable H pulse width(READ)		TEWHR		500	-	
CSB setup time	CSB	TCSS6		100	-	
CSB hold time		TCSH6		130	-	
WRITE Data setup time	D[7:0]	TDS6		200	-	
WRITE Data hold time		TDH6		250	-	
Read data access time		TACC6	CL=100pF	-	950	
Read data Output disable time		TOH6	CL=100pF	5	200	

Note:

1. The input signal rise time and fall time (tr,tf) is specifiedat15nsorless. When the system cycle time is extremely Fast,(tr+tf)≤(tCYC8 – tCCLW – tCCHW)for (tr+tf)≤(tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specifiedusing20%and80% of VDDI as the reference.
3. tCCLWandtCCLRarespecifiedastheoverlapbetweenCSBbeing “L” and/WR and/RD being at the “L” level. CSB and/WR(or/RD) cannot act at the same time and CSB should be 100ns widther than/WR(or/RD).

3.3.3 System Bus Timing for 4-Line Series Interface



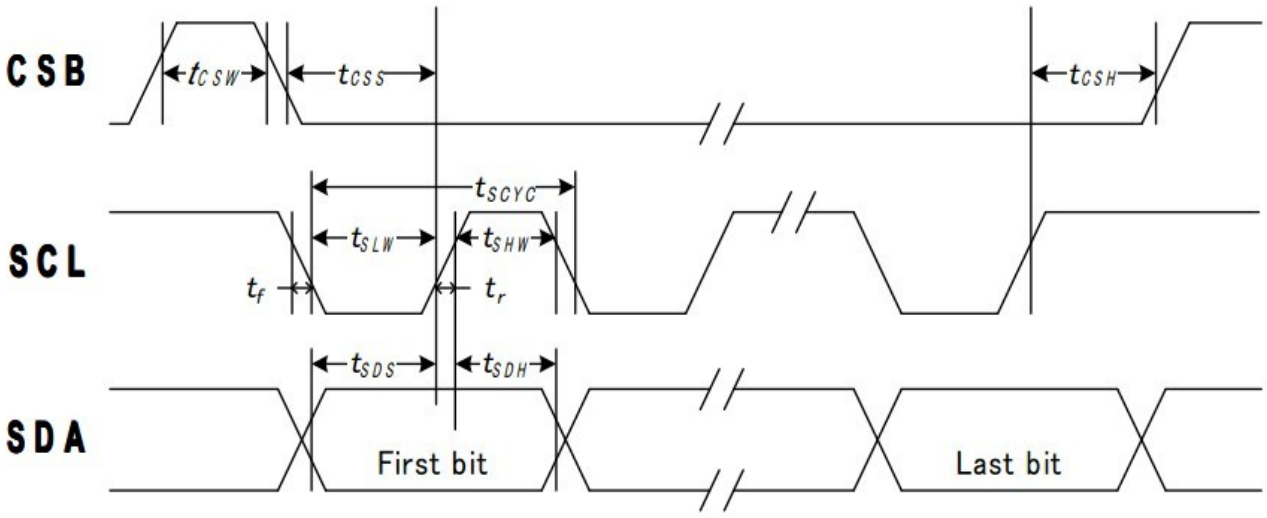
AGND=PGND=DGND=0V,VDDA=VDDP=VDDI=3.0~5.0V,Ta=25° C

Item	SIgnal	Symbol	Condition	Min	Max	Unit
Serial clock period	SCL	tSCYC		300	-	ns
SCL “H” pulse width		tSHW		150	-	
SCL “L” pulse width		tSLW		150	-	
Address setup time	AO	tSAS		150	-	
Address hold time		tSAH		150	-	
Data setup time	SDA	tSDS		120	-	
Data hold time		tSDH		120	-	
CSB -SCL time	CSB	tCSS		150	-	
CSB-SCL time		tCSH		150	-	
COB”H” Pulse width		tCSW		30	-	

Note:

1. The input signal rise and fall time (tr,tf)arespecifiedat15nsorless.
2. All timing is specifiedusing20%and80% of VDDI as the standard.

3.3.4 System Bus Timing for 3-Line Series Interface



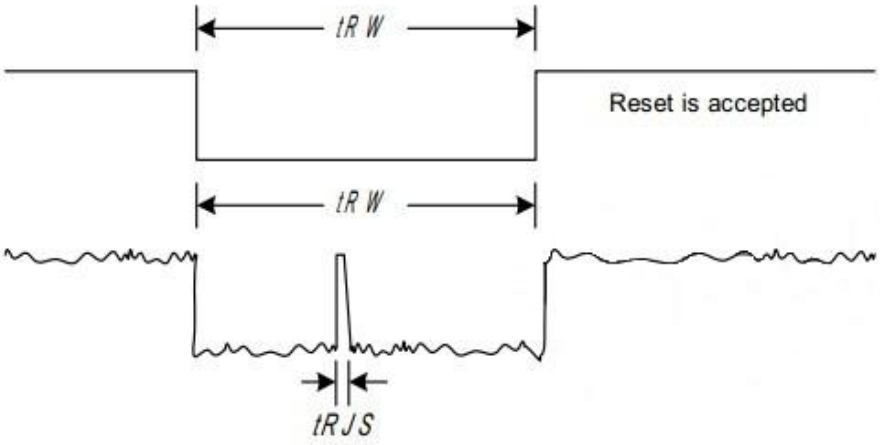
AGND=PGND=DGND=0V,VDDA=VDDP=VDDI=3.0~5.0V,Ta=25° C

Item	SIgnal	Symbol	Condition	Min	Max	Unit
Serial clock period	SCL	tSCYC		300	-	ns
SCL “H” pulse width		tSHW		150	-	
SCL “L” pulse width		tSLW		150	-	
Data setup time	SDA	tSDS		120	-	
Data hold time		tSDH		120	-	
CSB -SCL time	CSB	tCSS		150	-	
CSB-SCL time		tCSH		150	-	
COB”H” Pulse width		tCSW		30	-	

Note:

1. The input signal rise and fall time (tr,tf)arespecifiedat15nsorless.
2. All timing is specifiedusing20%and80% of VDDI as the standard.

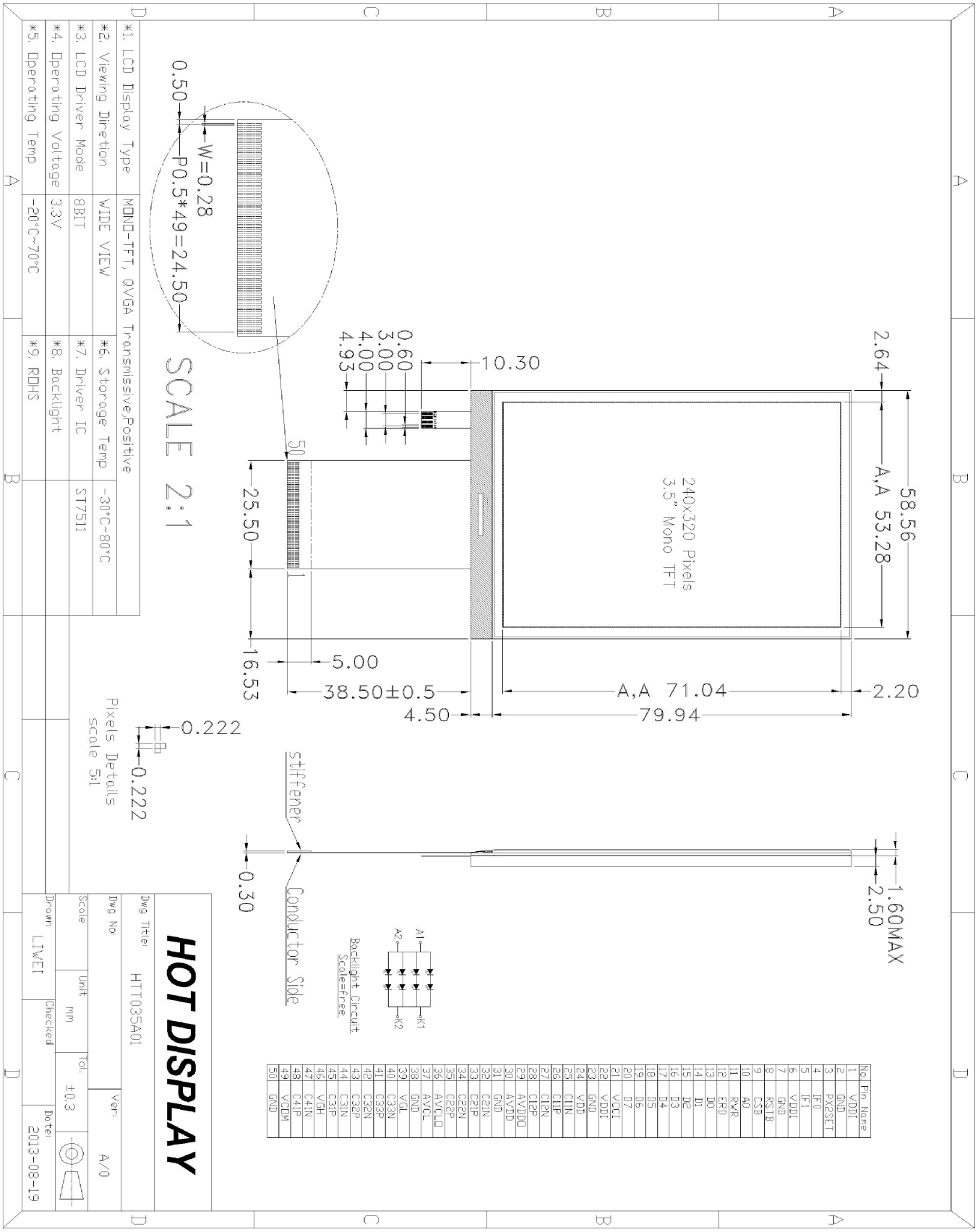
3.4 **Rest Timing**



Note:

1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do NOT use any PROM related command during this period
2. When the system issues a RSTB LOW pulse ,the reset procedure of IC will start if the LOW pulse is longer than tRW specifide above .if the LOW pulse is less than TRJ specifide above, the rest procedure of IC will not start. If the LOW pulse is longer than TRJ and less than TRW,the reset procedure of IC not guaranteed.

4. Structure Block



No.	Pin Name
1	VDDI
2	GND
3	PX2SET
4	IF0
5	IF1
6	VDDI
7	GND
8	RSTB
9	CSB
10	A0
11	RWR
12	ERD
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	VCI
22	VDDI
23	GND
24	VDD
25	C11N
26	C11P
27	C12N
28	C12P
29	AVDDO
30	AVDD
31	GND
32	C21N
33	C21P
34	C22N
35	C22P
36	AVCLO
37	AVCL
38	GND
39	VGL
40	C23N
41	C23P
42	C32N
43	C32P
44	C31N
45	C31P
46	VGH
47	C41N
48	C41P
49	VCOM
50	GND

4.1 Terminal Function

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Typ</th><th>Function</th></tr>
<tr><td>1</td><td>VDDI</td><td>O</td><td>Power Supply (3.3V)</td></tr>
<tr><td>2</td><td>GND</td><td>O</td><td>Ground</td></tr>
<tr><td>3</td><td>PX2SET</td><td>I</td><td>Select pin of AVDD pump multiplier
<table>
<tr><th>PX2SET</th><th>AVDD pump multiplier</th><th>Desctiption</th></tr>
<tr><td>H</td><td>X 2</td><td>VDDA=5.0V</td></tr>
<tr><td>L</td><td>X 3</td><td>VDDA=3.3V</td></tr>
</table></td></tr>
<tr><td>4</td><td>IF0</td><td rowspan="2">I</td><td rowspan="2">IF1 selects the interface mode (Serial or Parallel), and IF0 selects the microprocessor type in
parallel interface mode (8080-series or 6800-series).
<table>
<tr><th>IF1</th><th>IF0</th><th>Selected Interface</th></tr>
<tr><td>L</td><td>L</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>L</td><td>H</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>H</td><td>L</td><td>3-line serial interface</td></tr>
<tr><td>H</td><td>H</td><td>4-line serial interface</td></tr>
</table></td></tr>
<tr><td>5</td><td>IF1</td></tr>
<tr><td>6</td><td>VDDI</td><td></td><td>Power supply for IO system.</td></tr>
<tr><td>7</td><td>GND</td><td></td><td>VEE</td></tr>
<tr><td>8</td><td>RSTB</td><td>I</td><td>Reset input pin.Active when it is low.This pin is Effective when RSTEN pin is High.
Initialization is executed when this pin is set to Low.SWRESET command must be required after initialization.</td></tr>
<tr><td>9</td><td>CSB</td><td>I</td><td>Chip select input pin.
Interface access is enabled when CSB is “H”in Parallel ,SPI interface.
When CSB is non-active(CSB=“H”),D[7:0] pins are high impedance.</td></tr>
<tr><td>10</td><td>A0</td><td>I</td><td>Data /Command identification pin.
A0= Hi: Display data or parameter
A0=Low: Command
When using 3-line serial interface:
A0=Hi</td></tr>
<tr><td>11</td><td>RWR</td><td>I</td><td>Read /Write execution control pin.When IF1 is 0
<table>
<tr><th>IF0</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>1</td><td>6800 series</td><td>R/W</td><td>Read/ Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>0</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td></td><td></td><td></td><td>Edge of/ WR signal.</td></tr>
</table>
RWR is not used in serial interface and should fix to IF1 by VDDI.
</td></tr>
<tr><td>12</td><td>ERD</td><td>I</td><td>
Read/ Write execution control pin.When IF1 is 0
<table>
<tr><th>IF0</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>1</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”,D[7:0] are in output mode.
R/W=”L“:Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>0</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When/ RD is “L”, D[7:0] are in Output mode</td></tr>
</table>
ERD is not used in serial interface and should fix to“R3=0Ω”by VDDI.
</td></tr>
<tr><td>13~20</td><td>D0~D7</td><td>I/O</td><td>When using 8-bit parallel interface:(6800 or 8080 mode)8-bit bi-directional data bus.Connect to the data bus of 8-bit microprocessor.
When chip select pins are not active(CSB=“H”),D[7:0] pins are high impedance.
When using serial interface: 3-line or 4-line
D7: Serial input clock(SCL).
D0: Serial data (SDA).
D[6:1]: fix to“H”by VDDI.
When chip select pin (CSB) is not active,D[7:0] are high impedance</td></tr>
<tr><td>21</td><td>VCCI</td><td>I</td><td>Digital reference power voltage input</td></tr>
<tr><td>22</td><td>VDDI</td><td></td><td>Power supply for IO system.</td></tr>
<tr><td>23</td><td>GND</td><td></td><td>VEE</td></tr>
<tr><td>24</td><td>C11N</td><td rowspan="4">I/O</td><td rowspan="4">Flying Capacitor for generating AVDD Output
Connecting pins on the positive side. If 1st booster is not used, please open them.</td></tr>
<tr><td>25</td><td>C11P</td></tr>
<tr><td>26</td><td>C12N</td></tr>
<tr><td>28</td><td>C12P</td></tr>
<tr><td>29</td><td>AVDDO</td><td>O</td><td>Power pin for analog circuits. Connect to a capacitor for stabilization</td></tr>
<tr><td>30</td><td>AVDD</td><td>O</td><td>Power pin for analog circuits. Connect to a capacitor for stabilization</td></tr>
<tr><td>31</td><td>GND</td><td>O</td><td>VEE</td></tr>
<tr><td>32</td><td>C21N</td><td rowspan="4">I/O</td><td rowspan="4">Flying Capacitor for generating AVCL Output
Connecting pins on the positive side. If 2nd booster is not used, please open them.</td></tr>
<tr><td>33</td><td>C21P</td></tr>
<tr><td>34</td><td>C22P</td></tr>
<tr><td>35</td><td>C22P</td></tr>
<tr><td>36</td><td>AVCLO</td><td>O</td><td>Power supply pin for generating GVCL. Connect to a capacitor for stabilization.</td></tr>
<tr><td>37</td><td>AVCL</td><td>O</td><td>Power supply pin for generating GVCL. Connect to a capacitor for stabilization.</td></tr>
</table>

38	GND		VEE
39	VGL	O	Power supply pin for gate driver . Connect to a capacitor for stabilization
40	C33N	I/O	Flying Capacitor for generating VGL Output Connecting pins on the negative side.
41	C33P		
42	C32N		
43	C32P		
44	C31N		
45	C31P		
46	VGH	O	Power supply pin for gate driver . Connect to a capacitor for stabilization.
47	C41N	I/O	Flying Capacitor for generating VGH Output
48	C41P		
49	VCOM	O	Power supply for the TFT-LCD common electrode.
50	GND	O	VEE

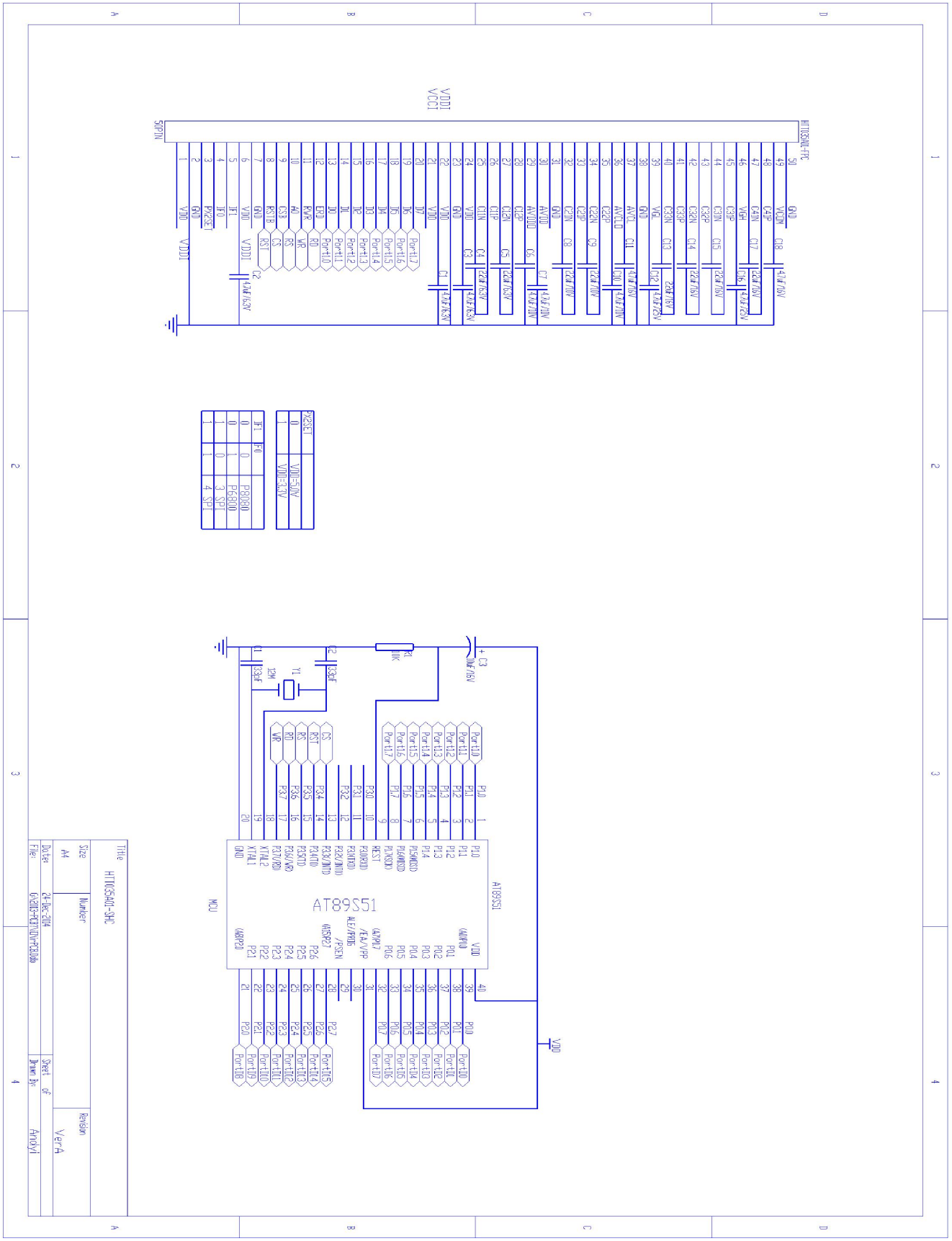
4.2 Interface selection

IF0	IF1	Selected Interface
L	L	8-bit 8080 parallel interface
H	L	8-bit 6800 parallel interface
L	H	3-line serial interface
H	H	4-line serial interface

4.3 Voltage selection

PX2SET	AVDD pump multiplier	Description
H	X2	VDDA=5.0V
L	X3	VDDA=3.3V

4.4. Interface specifications



5. Display Data RAM (DDRAM)

5.1 4bpp DDRAM Map

Page address		0	1	2	…	237	238	239	normal	Column address
normal	inert	239	238	237	…	2	1	0	invert	
0	159	D[0:3]	D[0:3]	D[0:3]	…	D[0:3]	D[0:3]	D[0:3]	G0	
		D[4:7]	D[4:7]	D[4:7]	…	D[4:7]	D[4:7]	D[4:7]	G1	
1	158	D[0:3]	D[0:3]	D[0:3]	…	D[0:3]	D[0:3]	D[0:3]	G2	
		D[4:7]	D[4:7]	D[4:7]	…	D[4:7]	D[4:7]	D[4:7]	G3	
…	…	…	…	…	…	…	…	…	…	
158	1	D[0:3]	D[0:3]	D[0:3]	…	D[0:3]	D[0:3]	D[0:3]	G316	
		D[4:7]	D[4:7]	D[4:7]	…	D[4:7]	D[4:7]	D[4:7]	G317	
159	0	D[0:3]	D[0:3]	D[0:3]	…	D[0:3]	D[0:3]	D[0:3]	G318	
		D[4:7]	D[4:7]	D[4:7]	…	D[4:7]	D[4:7]	D[4:7]	G319	
Source		S0	S1	S2	…	S237	S238	S239	Gate	

Gate	4bpp mode (>160 lines)		4bpp mode (<=160 lines)		2bpp mode		1bpp mode	
	Page address	Frame address	Page address	Frame address	Page address	Frame address	Page address	Frame address
G0	0	0	0	0/1	0	0/1	0	0/1/2/3
G1								
G2	1		1					
G3								
G4	2		2		1			
G5								
G6	3		3					
G7								
G8	4		4		2		1	
G9								
G230	155	0	155	0/1	77	0/1	38	0/1/2/3
G231								
G232	156		156		78		39	
G233								
G234	157		157					
G235								
G236	158		158		79			
G237								
G238	159		159					
G239								

6. Commands Descriptions

6.1 Software Reset

AEH	Software Reset											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	1	↑	1	0	1	0	1	1	1	0	AE
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	. This command make a reset as same ad hardware . . It is required Hardware reset at power-on reset .It is always required to input this command after hardware reset											

6.2 Power Control

61H	Power Control											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTL	0	1	↑	0	1	1	0	0	0	0	0	61
1st parameter	1	1	↑	BST3SR1	BST3SR0	0	0	FOF4ON	FOF3ON	FOF2ON	FOF1ON	40
2nd parameter	1	1	↑	FOFNO3	FOFNO2	FOFNO1	FOFNO0	0	SAMPSet2	SAMPSet1	SAMPSet0	04
3rd parameter	1	1	↑	0	0	1	0	0	0	1	0	02
4th parameter	1	1	↑	1	0	0	0	0	1	0	1	A5
Description	. Booster circuit control, source amp setting and booster clock frequency settings. . This command must be input before SLPOUT command. . BST3SR[1:0]: Step-up rate of the 3rd booster setting 00,01:"-1" 10:"-2" 11:"-3" . BST4ON~BST1ON:4th~1st booster On/OFF setting 0:Booster off 1:Booster on . FOFNo[3:0]: Force off frame, set waiting time by number of frames from sleep out to display on. . SAMPSst[2:0]: Source amplifier setting											

6.3 Electronic Volumn Set 1

62H	Electronic Volumn Set 1											
Ins/Pat	**A1**	**ERD**	**RER**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
EVSWT1	0	1	↑	0	1	1	0	0	0	1	0	62
1st parameter	1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A
2nd parameter	1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06
3rd parameter	1	1	↑	0	0	1	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	0F
4th parameter	1	1	↑	1	0	0	0	0	1	0	1	A5

Description

. Set each output voltages of built in voltage regulators

. VGL and VGH are determined by VGHREG and VGLREG . (refer to 6.5)

VCOM[6:0]	VCOM(V)
00h	-0.3000
01h	-0.3125
02h	-0.3250
03h	-0.3375
...	....
3Dh	-1.6025
3Eh	-1.0750
3Fh	-1.0875
....	...
7Dh	-1.8625
7Eh	-1.8750
7Fh	-1.8875

VGHREG[5:0]	VGHREG(V)
00h	0
01h	1.5
02h	1.6
03h	1.7
...	...
2Eh	6.0
2Fh	6.1
30h	6.2
31h	6.2
...	...
3Eh	6.2
3Fh	6.2

VGHREG[4:0]	VGHREG(V)
00h	2.4
01h	2.5
02h	2.6
03h	2.7
...	...
1Dh	5.3
1Eh	5.4
1Fh	5.5

6.4 Display Set 2

33H	Display Set 2											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISAR	0	1	↑	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A
2nd parameter	1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	28
3rd parameter	1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C
4th parameter	1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	26
Description	. Set source and gate ON/OFF timing . SOnT: Set source on timing by “number of clock from start-1” . SOffT: Set source off timing by “number of clock from start-1” . SOnT: Set source on timing by “number of clock from start-1” . SOffT: Set source off timing by “number of clock from start-1”											

6.5 Electronic Volumn Set 2

63H	Electronic Volumn Set 1											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EVSET2	0	1	↑	0	1	1	0	0	0	1	0	63
1st parameter	1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F
2nd parameter	1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F
3rd parameter	1	1	↑	1	0	1						A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description: . Set each output voltages of built in voltage regulators

VCOM[6:0]	VCOM(V)
00h	-0.3000
01h	-0.3125
02h	-0.3250
03h	-0.3375
...	....
3Dh	-1.6025
3Eh	-1.0750
3Fh	-1.0875
....	...
7Dh	-1.8625
7Eh	-1.8750
7Fh	-1.8875

VGHREG[5:0]	VGHREG(V)
00h	0
01h	1.5
02h	1.6
03h	1.7
...	...
2Eh	6.0
2Fh	6.1
30h	6.2
31h	6.2
...	...
3Eh	6.2
3Fh	6.2

6.6 Memory Address Control

24H	Memory Address Control											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	1	↑	0	0	1	0	0	1	0	0	24
1st parameter	1	1	↑	0	0	0	0	0	MV	MY	MX	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set about display data TAM. ▪ To access display RAM, it is required 1ms or more wait after input this command. ▪ MV: Select address incremental direction.(refer to 6.) 0: Incremental column addr . 1:Incremental page addr. ▪ MY: Display data RAM page address (refer to 6.) 0: Normal 1: Reverse ▪ MX: Display data RAM column address (refer to 6.). 0: Normal 1: Reverse											

6.7 BPP Select

22H	BPP Selection											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPPSEL	0	1	↑	0	0	1	0	0	0	1	0	22
1st parameter	1	1	↑	0	0	0	0	0	0	Bppsel1	Bppsel0	02
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set data format (bit per pixel) ▪ It is enabled next frame after receiving the command. ▪ It is possible to change 4bpp / 2bpp / 1bpp. ▪ It must be input during display off state, and display data must be written after changing ▪ BppSel[1:0] : Set data format (bit per pixel) 00: 1bpp (2 gray scale) 01: 2bpp (4 gray scale) 10: 4bpp (16 gray scale)											

6.8 Gamma Set 4bpp Positive 1

91H	Gamma Set 4bpp Positive 1											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P1	0	1	↑	0	0	0	1	0	0	0	1	91
1st parameter	1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00
2nd parameter	1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04
3rd parameter	1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08
4th parameter	1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	0C
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV0: V0 voltage setting (positive polarity) ▪ G4BPV1: V1 voltage setting (positive polarity) ▪ G4BPV2: V2 voltage setting (positive polarity) ▪ G4BPV3: V3 voltage setting (positive polarity)											

6.9 Gamma Set 4bpp Positive 2

92H	Gamma Set 4bpp Positive 2											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P2	0	1	↑	1	0	0	1	0	0	1	0	92
1st parameter	1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10
2nd parameter	1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14
3rd parameter	1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18
4th parameter	1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV4: V4 voltage setting (positive polarity) ▪ G4BPV5: V5 voltage setting (positive polarity) ▪ G4BPV6: V6 voltage setting (positive polarity) ▪ G4BPV7: V7 voltage setting (positive polarity)											

6.10 Gamma Set 4bpp Positive 3

93H	Gamma Set 4bpp Positive 3											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P3	0	1	↑	1	0	0	1	0	0	1	1	93
1st parameter	1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23
2nd parameter	1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27
3rd parameter	1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B
4th parameter	1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV8: V8 voltage setting (positive polarity) ▪ G4BPV9: V9 voltage setting (positive polarity) ▪ G4BPV10: V10 voltage setting (positive polarity) ▪ G4BPV11: V11 voltage setting (positive polarity)											

6.11 Gamma Set 4bpp Positive 4

94H	Gamma Set 4bpp Positive 4											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P4	0	1	↑	1	0	0	1	0	0	1	1	94
1st parameter	1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33
2nd parameter	1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37
3rd parameter	1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B
4th parameter	1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV12: V12 voltage setting (positive polarity) ▪ G4BPV13: V13voltage setting (positive polarity) ▪ G4BPV14: V14voltage setting (positive polarity) ▪ G4BPV15: V15 voltage setting (positive polarity)											

6.12 Sleep Out

12H	Sleep Out											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	1	↑	0	0	0	1	0	0	1	0	12
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ This command make a reset as same as hardware reset. ▪ It is required hardware reset at power-on. ▪ It is always required to input this command after hardware reset.											

Sleep In

13H	Sleep Out											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	1	↑	0	0	0	1	0	0	1	1	13
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

6.13 Display On

15H	Display On											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISON	0	1	↑	0	0	0	1	0	1	0	1	15
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Start to display. ▪ SLPOUT command must be input before this command. ▪ After SLPOUT command, DISON command is waited until “display possible state” and this command is executed after wait time set by PWRCTL command.											

Display Off

15H	Display On											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISOFF	0	1	↑	0	0	0	1	0	1	0	1	14
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

6.14 Page Address Set

25H	Page Address Set											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PASET	0	1	↑	0	0	1	0	0	1	0	1	25
1st parameter	1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00
2nd parameter	1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	9F
3rd parameter	1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set page start address and page end address of display data RAM. ▪ PSA: Set page START address ▪ PEA: Set page END address ▪ FrmA: Set frame address ▪ Frame address range set by PASET command is depend on setting of BPPSEL command ▪ PSA < PEA											

6.15 Column Address Set

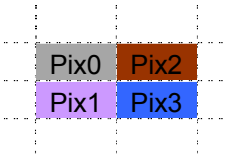
26H	Column Address Set											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	1	↑	0	0	1	0	0	1	1	0	26
1st parameter	1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00
2nd parameter	1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00
3rd parameter	1	1	↑	0	0	0	0	0	0			02
4th parameter	1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F
Description	▪ Set column start address and column end address of display data RAM. ▪ CSA: Set column START address ▪ CEA: Set column END address ▪ CSA < CEA											

6.16 Write RAM

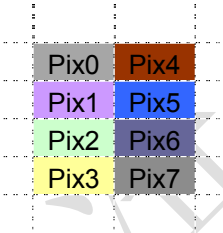
2CH	Write RAM											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRRAM	0	1	↑	0	0	1	0	0	1	0	0	2C
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Write data	1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	
Description	▪ After this WRRAM command, data is input at display area which is set by CASET and PASET command. ▪ RAM address is incremented automatically by WR signal. ▪ Column address, page address and frame address are set to start addresses by WRRAM command input.											

6.17 Addressing

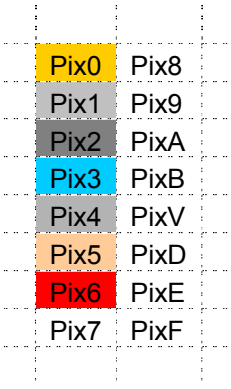
4bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DDRAM write	0	0	0	1	0	1	1	0	0	2C
command	1	1	0	0	0	0	1	0	1	00
1st write	1	Pix13	Pix12	Pix11	Pix10	Pix03	Pix02	Pix01	Pix00	xx
2nd write	1	Pix33	Pix32	Pix31	Pix30	Pix23	Pix22	Pix21	Pix20	xx



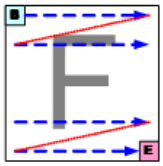
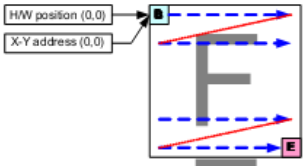
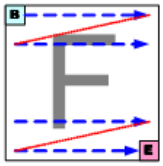
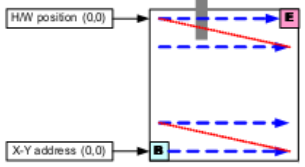
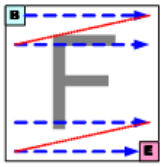
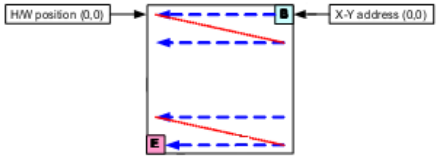
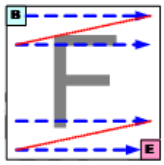
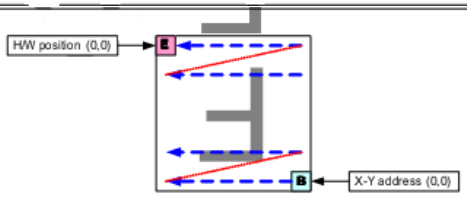
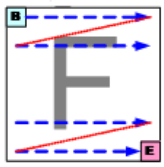
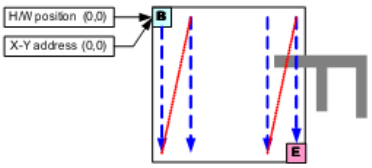
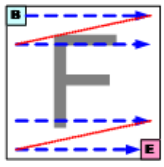
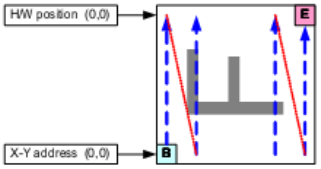
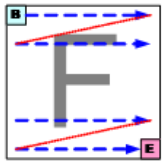
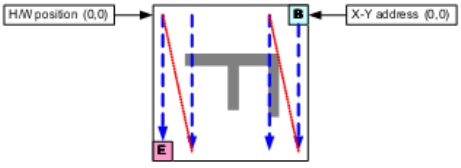
2bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DDRAM write	0	0	0	1	0	1	1	0	0	2C
command	1	1	0	0	0	0	1	0	1	00
1st write	1	Pix31	Pix30	Pix21	Pix20	Pix11	Pix10	Pix01	Pix00	xx
2nd write	1	Pix71	Pix70	Pix61	Pix60	Pix51	Pix50	Pix41	Pix40	xx

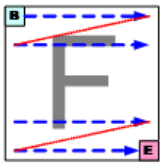
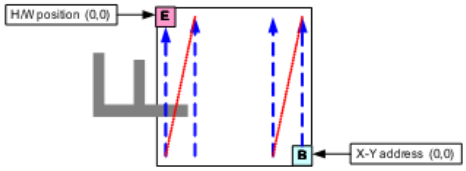


1bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DDRAM write	0	0	0	1	0	1	1	0	0	2C
command	1	1	0	0	0	0	1	0	1	00
1st write	1	Pix7	Pix6	Pix5	Pix4	Pix3	Pix2	Pix1	Pix0	xx
2nd write	1	PixF	PixE	PixD	PixC	PixB	PixA	Pix9	Pix8	xx



7. Page Address Circuit and Column Address Circuit

Display data direction	Memory access control			Image in the host	Image in the driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		

X-Y Exchange X-Mirror Y-Mirror	1	1	1		

8. Command Table

Instruction	Add. (hex)	A0	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	Function
NOP	00	0	1	↑	0	0	0	0	0	0	0	0		Non-Operation
		1	1	↑	1	0	1	0	0	1	0	1		
SLPOUT	12	0	1	↑	0	0	0	1	0	0	1	0		Sleep Out
		1	1	↑	1	0	1	0	0	1	0	1		
SLPIN	13	0	1	↑	0	0	0	1	0	0	1	1		Sleep In
		1	1	↑	1	0	1	0	0	1	0	1		
DISOFF	14	0	1	↑	0	0	0	1	0	1	0	0		Display Off
		1	1	↑	1	0	1	0	0	1	0	1		
DISON	15	0	1	↑	0	0	0	1	0	1	0	1		Display On
		1	1	↑	1	0	1	0	0	1	0	1		
DINVOUT	1A	0	1	↑	0	0	0	1	1	0	1	0		Display
		1	1	↑	1	0	1	0	0	1	0	1		Invert Out
DINVIN	1B	0	1	↑	0	0	0	1	1	0	1	1		Display
		1	1	↑	1	0	1	0	0	1	0	1		Invert In
BLOUT	1C	0	1	↑	0	0	0	1	1	1	0	0		Blinking Out
		1	1	↑	1	0	1	0	0	1	0	1		
BLIN	1D	0	1	↑	0	0	0	1	1	1	0	1		Blinking In
		1	1	↑	1	0	1	0	0	1	0	1		
STFRAME	21	0	1	↑	0	0	1	0	0	0	0	1		Start Frame Address
		1	1	↑	0	0	0	0	0	0	SFrmA1	SFrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BPPSEL	22	0	1	↑	0	0	1	0	0	0	1	0		BPP Select
		1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MADCTL	24	0	1	↑	0	0	1	0	0	1	0	0		Memory Address Control
		1	1	↑	0	0	0	0	0	MV	MY	MX	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PASET	25	0	1	↑	0	0	1	0	0	1	0	1		Page Address Set
		1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00	
		1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	9F	
		1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
CASET	26	0	1	↑	0	0	1	0	0	1	1	0		Column

		1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00	Address Set
		1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00	
		1	1	↑	0	0	0	0	0	0	CEA9	CEA8	02	
		1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F	
BLKFIL	29	0	1	↑	0	0	1	0	1	0	0	1		Block Fill
		1	1	↑	0	0	0	0	BFData3	BFData2	BFData1	BFData0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BLSET	2B	0	1	↑	0	0	1	0	1	0	1	1		Blinking Set
		1	1	↑	BlinkCyc7	BlinkCyc6	BlinkCyc5	BlinkCyc4	BlinkCyc3	BlinkCyc2	BlinkCyc1	BlinkCyc0	1D	
		1	1	↑	0	0	0	0	B1stF1	B1stF0	B2ndF1	B2ndF0	01	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
WRRAM	2C	0	1	↑	0	0	1	0	1	1	0	0		Write RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
RDRAM	2D	0	1	↑	0	0	1	0	1	1	0	1		Read RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	X	X	X	X	X	X	X	X		
		1	↑	1	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
DISAR	31	0	1	↑	0	0	1	1	0	0	0	1		Display Area
		1	1	↑	0	0	0	0	0	0	0	DisLin8	01	
		1	1	↑	DisLin7	DisLin6	DisLin5	DisLin4	DisLin3	DisLin2	DisLin1	DisLin0	3F	
		1	1	↑	0	0	0	0	0	0	1	0	02	
		1	1	↑	0	1	1	1	1	1	1	1	7F	
DISSET1	32	0	1	↑	0	0	1	1	0	0	1	0		Display Set1
		1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	32	
		1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0	02	
		1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	00	
		1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	01	
DISSET2	33	0	1	↑	0	0	1	1	0	0	1	1		Display Set2
		1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A	
		1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	28	
		1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C	
		1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	26	
PTLSET1	34	0	1	↑	0	0	1	1	0	1	0	0		Partial Set 1
		1	1	↑	0	0	0	0	0	0	0	Part1SL8	00	
		1	1	↑	Part1SL7	Part1SL6	Part1SL5	Part1SL4	Part1SL3	Part1SL2	Part1SL1	Part1SL0	00	
		1	1	↑	0	0	0	0	0	0	0	Part1EL8	00	
		1	1	↑	Part1EL7	Part1EL6	Part1EL5	Part1EL4	Part1EL3	Part1EL2	Part1EL1	Part1EL0	00	
PTLSET2	35	0	1	↑	0	0	1	1	0	1	0	1		Partial Set 2
		1	1	↑	0	0	0	0	0	0	0	Part2SL8	00	
		1	1	↑	Part2SL7	Part2SL6	Part2SL5	Part2SL4	Part2SL3	Part2SL2	Part2SL1	Part2SL0	00	
		1	1	↑	0	0	0	0	0	0	0	Part2EL8	00	

		1	1	↑	Part2EL7	Part2EL6	Part2EL5	Part2EL4	Part2EL3	Part2EL2	Part2EL1	Part2EL0	00	
PTLSET3	36	0	1	↑	0	0	1	1	0	1	1	0		Partial Set 3
		1	1	↑	0	NDisRefR6	NDisRefR5	NDisRefR4	NDisRefR3	NDisRefR2	NDisRefR1	NDisRefR0	00	
		1	1	↑	0	0	0	0	0	RTBFreq2	RTBFreq1	RTBFreq0	00	
		1	1	↑	0	0	0	0	0	0	NDisDM1	NDisDM0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
VCMDAT	54	0	1	↑	0	1	0	1	0	1	0	0		VCOM Offset Data
		1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	00	
		1	1	↑	0	0	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00	
		1	1	↑	0	0	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	00	
		1	1	↑	1	0	1	0	0	1	0	1		
UIDSET	55	0	1	↑	0	1	0	1	0	1	0	1		User ID
		1	1	↑	UID117	UID116	UID115	UID114	UID113	UID112	UID111	UID110	00	
		1	1	↑	UID127	UID126	UID125	UID124	UID123	UID122	UID121	UID120	00	
		1	1	↑	UID217	UID216	UID215	UID214	UID213	UID212	UID211	UID210	00	
		1	1	↑	UID227	UID226	UID225	UID224	UID223	UID222	UID221	UID220	00	
MTPMOD	5A	0	1	↑	0	1	0	1	1	0	1	0		Multi Time PROM Mode
		1	1	↑	MTPMOD7	MTPMOD6	MTPMOD5	MTPMOD4	MTPMOD3	MTPMOD2	MTPMOD1	MTPMOD0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MTPOP	5B	0	1	↑	0	1	0	1	1	0	1	1		Multi Time PROM Operation
		1	1	↑	0	0	0	0	0	MTP_Sel	0	Prog_Mod	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWRCTL	61	0	1	↑	0	1	1	0	0	0	0	1		Power Control
		1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON	40	
		1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	04	
		1	1	↑	0	0	0	0	0	0	1	0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET1	62	0	1	↑	0	1	1	0	0	0	1	0		Electronic Volumn Set 1
		1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A	
		1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06	
		1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET2	63	0	1	↑	0	1	1	0	0	0	1	1		Electronic Volumn Set 2
		1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F	
		1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BCLKSET	64	0	1	↑	0	1	1	0	0	1	0	0		Booster Clock Setting
		1	1	↑	0	AVclClk2	AVclClk1	AVclClk0	0	AVdClk2	AVdClk2	AVdClk2	44	
		1	1	↑	0	VglClk2	VglClk1	VglClk0	0	Vghclk2	Vghclk1	VghClk0	44	
		1	1	↑	0	AVdClk_nd2	AVdClk_nd1	AVclClk_nd2	0	AVdClk_nd2	AVdClk_nd1	AVdClk_nd0	44	

		1	1	↑	0	VglClk_nd2	VglClk_nd1	VglClk_nd0	0	Vghdlk_nd2	Vghdlk_nd1	VghClk_nd0	44	
GATESET	66	0	1	↑	0	1	1	0	0	1	1	0		Gate Set
		1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWMCTRL	6C	0	1	↑	0	1	1	0	1	1	0	0		PWM Control
		1	1	↑	0	0	0	0	0	LOnTyp	0	LEDMD	00	
		1	1	↑	SLEDOn7	SLEDOn6	SLEDOn5	SLEDOn4	SLEDOn3	SLEDOn2	SLEDOn1	SLEDOn0		
		1	1	↑	ASLEDOn7	ASLEDOn6	ASLEDOn5	ASLEDOn4	ASLEDOn3	ASLEDOn2	ASLEDOn1	ASLEDOn0		
		1	1	↑	ASLEDOf7	ASLEDOf6	ASLEDOf5	ASLEDOf4	ASLEDOf3	ASLEDOf2	ASLEDOf1	ASLEDOf0		
RDSTAT	72	0	1	↑	0	1	1	1	0	0	1	0		Read Status
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	0	R13	R12	R11	R10		
		1	↑	1	0	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	0	0	0	0	0	R52	R51	R50		
		1	↑	1	0	R66	R65	R64	0	R62	R61	R60		
RDREV	73	0	1	↑	0	1	1	1	0	0	1	1		Read Revision
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
RDUID	75	0	1	↑	0	1	1	1	0	1	0	1		Read User ID
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50		
		1	↑	1	R67	R66	R65	R64	R63	R62	R61	R60		
		1	↑	1	R77	R76	R75	R74	R73	R72	R71	R70		
		1	↑	1	R87	R86	R85	R84	R83	R82	R81	R80		
		1	↑	1	R97	R96	R95	R94	R93	R92	R91	R90		
		1	↑	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0		
		1	↑	1	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0		
		1	↑	1	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0		
RDVCMDAT	79	0	1	↑	0	1	1	1	1	0	0	1		Read VCOM Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	x	x	R15	R14	R13	R12	R11	R10		
		1	↑	1	x	x	R25	R24	R23	R22	R21	R20		
		1	↑	1	x	x	R35	R34	R33	R32	R31	R30		
		1	↑	1	x	x	R45	R44	R43	R42	R41	R40		
		1	↑	1	x	x	R55	R54	R53	R52	R51	R50		
		1	↑	1	x	x	R65	R64	R63	R62	R61	R60		
		1	↑	1	x	x	R75	R74	R73	R72	R71	R70		

		1	↑	1	0	0	0	0	R83	R82	R81	R80		
GAMSET4 P1	91	0	1	↑	1	0	0	1	0	0	0	1		Gamma Set 4bpp Positive 1
		1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00	
		1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04	
		1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08	
		1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	0C	
GAMSET4 P2	92	0	1	↑	1	0	0	1	0	0	1	0		Gamma Set 4bpp Positive 2
		1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10	
		1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14	
		1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18	
		1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C	
GAMSET4 P3	93	0	1	↑	1	0	0	1	0	0	1	1		Gamma Set 4bpp Positive 3
		1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23	
		1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27	
		1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B	
		1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F	
GAMSET4 P4	94	0	1	↑	1	0	0	1	0	1	0	0		Gamma Set 4bpp Positive 4
		1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33	
		1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37	
		1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B	
		1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F	
GAMSET2 P	95	0	1	↑	1	0	0	1	0	1	0	1		Gamma Set 2bpp Positive
		1	1	↑	0	0	G2BPV05	G2BPV04	G2BPV03	G2BPV02	G2BPV01	G2BPV00	00	
		1	1	↑	0	0	G2BPV15	G2BPV14	G2BPV13	G2BPV12	G2BPV11	G2BPV10	15	
		1	1	↑	0	0	G2BPV25	G2BPV24	G2BPV23	G2BPV22	G2BPV21	G2BPV20	2A	
		1	1	↑	0	0	G2BPV35	G2BPV34	G2BPV33	G2BPV32	G2BPV31	G2BPV30	3F	
GAMSET1	96	0	1	↑	1	0	0	1	0	1	1	0		Gamma Set 1bpp
		1	1	↑	0	0	G1BPV05	G1BPV04	G1BPV03	G1BPV02	G1BPV01	G1BPV00	00	
		1	1	↑	0	0	G1BPV15	G1BPV14	G1BPV13	G1BPV12	G1BPV11	G1BPV10	3F	
		1	1	↑	0	0	G1BNV05	G1BNV04	G1BNV03	G1BNV02	G1BNV01	G1BNV00	00	
		1	1	↑	0	0	G1BNV15	G1BNV14	G1BNV13	G1BNV12	G1BNV11	G1BNV10	3F	
GAMSET4 N1	99	0	1	↑	1	0	0	1	1	0	0	1		Gamma Set 4bpp Negative 1
		1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00	
		1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	04	
		1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	08	
		1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	0C	
GAMSET4 N2	9A	0	1	↑	1	0	0	1	1	0	1	0		Gamma Set 4bpp Negative 2
		1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	10	
		1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	14	
		1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	18	
		1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1C	
GAMSET4 N3	9B	0	1	↑	1	0	0	1	1	0	1	1		Gamma Set 4bpp Negative 3
		1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	23	
		1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	27	
		1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	2B	

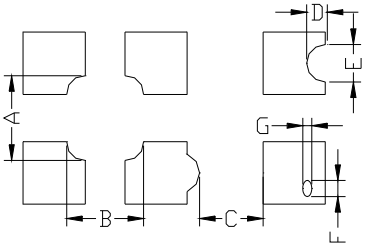
		1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F	
GAMSET4N4	9C	0	1	↑	1	0	0	1	1	1	0	0		Gamma Set 4bpp Negative 4
		1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33	
		1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	37	
		1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B	
		1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F	
GAMSET2N	9D	0	1	↑	1	0	0	1	1	1	0	1		Gamma Set 2bpp Negative
		1	1	↑	0	0	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00	
		1	1	↑	0	0	G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15	
		1	1	↑	0	0	G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A	
		1	1	↑	0	0	G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F	
RMWIN	A1	0	1	↑	1	0	1	0	0	0	0	1		Read Modify Write In
		1	1	↑	1	0	1	0	0	1	0	1		
MTPRDEN	A2	0	1	↑	1	0	1	0	0	0	1	0		MTP Read Enable
		1	1	↑	1	0	1	0	0	1	0	1		
MTPWREN	A3	0	1	↑	1	0	1	0	0	0	1	1		MTP Write Enable
		1	1	↑	1	0	1	0	0	1	0	1		
PTLOUT	A9	0	1	↑	1	0	1	0	1	0	0	1		Partial Out
		1	1	↑	1	0	1	0	0	1	0	1		
PTLIN	AA	0	1	↑	1	0	1	0	1	0	1	0		Partial In
		1	1	↑	1	0	1	0	0	1	0	1		
RMWOUT	AC	0	1	↑	1	0	1	0	1	1	0	0		Read Modify Write Out
		1	1	↑	1	0	1	0	0	1	0	1		
SWRESET	AE	0	1	↑	1	0	1	0	1	1	1	0		Software Reset
		1	1	↑	1	0	1	0	0	1	0	1		

9. Basic Operating Sequence

```
void Lcd_Init(void)
{
    RES=0;
    delay(10);
    RES=1;
    Comwrite(0xAE);
    Datawrite(0xA5);//software Reset
    delay(200);

    Comwrite(0x61);//POWER CONTROL 61PG
    Datawrite(0x8F);//
    Datawrite(0x04);
    Datawrite(0xA5);//
    Datawrite(0xA5);

    Comwrite(0x62);//-- VCOM/VGH/VGL default setting
    Datawrite(0x36);//
    Datawrite(0x0B);
    Datawrite(0x0B);//
    Datawrite(0xA5);

    Comwrite(0x33);// Source&Gate on/off fine tuning
    Datawrite(0x07);//
    Datawrite(0x2C);
```

```
    Datawrite(0x09);//
    Datawrite(0x2A);

    Comwrite(0x63);// -- GVDD/GVCL
    Datawrite(0x09);//
    Datawrite(0x17);
    Datawrite(0xA5);//
    Datawrite(0xA5);

   Comwrite(0x24);       //MV MY MX
    Datawrite(0x01);
    Datawrite(0xa5);
    Datawrite(0xa5);
    Datawrite(0xa5);

 /*   Comwrite(0x22);//Gray Select（Mono Mode)
    Datawrite(0x00);//
    Datawrite(0xA5);
    Datawrite(0xA5);//
    Datawrite(0xA5);   */

    Comwrite(0x91);
    Datawrite(0x00); //0
    Datawrite(0x17); //1//13 19
    Datawrite(0x1b); //2//15   1b
    Datawrite(0x1d); //3//16   1c

    Comwrite(0x92);
    Datawrite(0x1f); //4//18    1e
    Datawrite(0x21); //5//19    1f
    Datawrite(0x23); //6//1B
    Datawrite(0x25); //7//1C

    Comwrite(0x93);
    Datawrite(0x27); //8 //1E
    Datawrite(0x29); //9 //20
    Datawrite(0x2a); //10//23
    Datawrite(0x2c); //11//25

    Comwrite(0x94);
    Datawrite(0x2e); //12//27
    Datawrite(0x31); //13//2B
    Datawrite(0x34); //14//34
    Datawrite(0x3f); //15//3F

    Comwrite(0x99);
    Datawrite(0x00); //0
    Datawrite(0x17); //1//13 19
    Datawrite(0x1b); //2//15   1b
    Datawrite(0x1d); //3//16   1c

    Comwrite(0x9a);
    Datawrite(0x1f); //4//18    1e
    Datawrite(0x21); //5//19    1f
    Datawrite(0x23); //6//1B
    Datawrite(0x25); //7//1C

    Comwrite(0x9b);
    Datawrite(0x27); //8 //1E
    Datawrite(0x29); //9 //20
    Datawrite(0x2a); //10//23
    Datawrite(0x2c); //11//25

    Comwrite(0x9c);
    Datawrite(0x2e); //12//27
    Datawrite(0x31); //13//2B
    Datawrite(0x34); //14//34
    Datawrite(0x3f); //15//3F

    Comwrite(0x12);       //-- SLP out
    Datawrite(0xa5);

    Comwrite(0x15);       //-- Display out
    Datawrite(0xa5);

   delay(10);

}
```

10. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28$ | $0<C$ | $\frac{D+E}{2}\leq 0.25$ | $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

11. Handling Precautions

11.1Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

11.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

11.3Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

11.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

11.5Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

11.6Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

11.7Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.

12. Packaging Specifications

鑫洪泰 HOT DISPLAY	Packaging Specifications HTT035A01	Approved	Checked	Designed

12.1 Packaging Material

No	Item	Dimensions(mm)	1PCS Weight(KG)	Quantity	Total Weight	
1	COG	58.56*79.94*4.1	0.050	200	10.0	
2	PE Bag	120*80	0.001	200	0.2	
3	Foam Rubber Cushion	310*170	0.0175	12	0.21	
4	Partition A1	310*170*100	0.30	6	1.8	
5	Product Box	330*180*120(neutral packing)	0.45	6	2.7	
6	Carton	480*390*330(neutral packing)	0.9	1	0.9	
7	Tape			AR		
8	Label Specifications			1		
9	Label Rohs			1		
10	Label ESD			1		

12.2. Total LCD Weight in carton: 15.8 KG±10%

12.3. Packaging Specifications and Quantity:

(1)Quantity Of Spacer:A1*4

(2)Total LCM quantity in carton: quantity per box 50* no of boxes 4 = 200