MR25H256

256Kb Serial SPI MRAM

FEATURES

- No write delays
- Unlimited write endurance
- Data retention greater than 20 years
- Automatic data protection on power loss
- Block write protection
- Fast, simple SPI interface with up to 40 MHz clock rate
- 2.7 to 3.6 Volt power supply range
- Low current sleep mode
- Industrial temperatures
- Small footprint 8-pin DFN RoHS-compliant package
- Direct replacement for serial EEPROM, Flash, FeRAM

INTRODUCTION

The **MR25H256** is a 262,144-bit magnetoresistive random access memory (MRAM) device organized as 32,768 words of 8 bits. The **MR25H256** offers serial EEPROM and serial Flash compatible read/write timing with no write delays and unlimited read/write endurance.

Unlike other serial memories, both reads and writes can occur randomly in memory with no delay between writes. The **MR25H256** is the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of I/O pins.

The **MR25H256** is available in a small footprint 5 mm x 6 mm 8-pin DFN package that is compatible with serial EEPROM, Flash, and FeRAM products.

The **MR25H256** provides highly reliable data storage over a wide range of temperatures. The product is offered with industrial temperature (-40° to +85 °C) options.

CONTENTS

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1. DEVICE PIN ASSIGNMENT

Overview

The MR25H256 is a serial MRAM with memory array logically organized as 32Kx8 using the four pin interface of chip select (CS), serial input (SI), serial output (SO) and serial clock (SCK) of the serial peripheral interface (SPI) bus. Serial MRAM implements a subset of commands common to today's SPI EEPROM and Flash components allowing MRAM to replace these components in the same socket and interoperate on a shared SPI bus. Serial MRAM offers superior write speed, unlimited endurance, low standby & operating power, and more reliable data retention compared to available serial memory alternatives.

Figure 1.1 Block Diagram
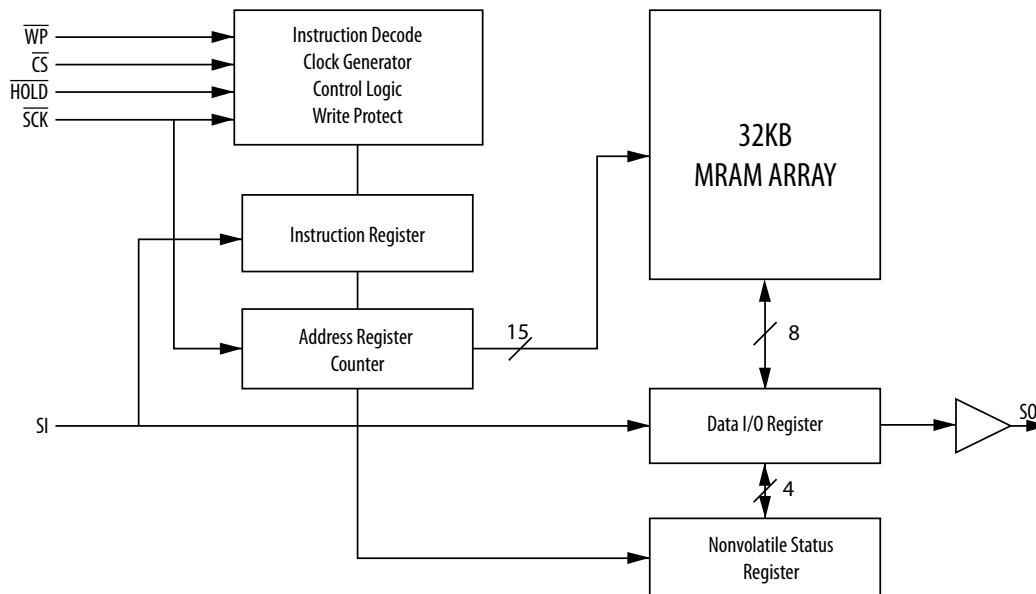
System Configuration

Single or multiple devices can be connected to the bus as show in Figure 1.2. Pins SCK, SO and SI are common among devices. Each device requires $\overline{CS}$ and $\overline{HOLD}$ pins to be driven seperately.

Figure 1.2 System Configuration
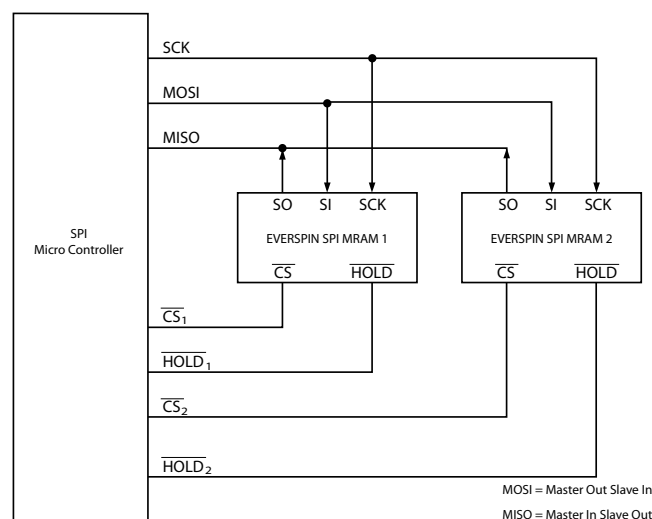
Figure 1.3 Pin Diagrams (Top View)

$\overline{CS}$	1 ○	8	V_{DD}
SO	2	7	$\overline{HOLD}$
$\overline{WP}$	3	6	SCK
V_{SS}	4	5	SI
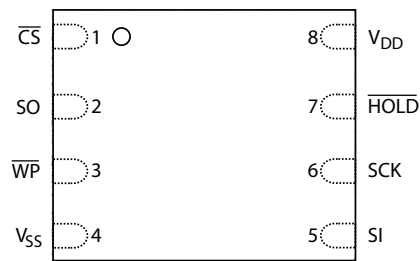
8-Pin DFN

Table 1.1 Pin Functions

Signal Name	Pin	I/O	Function	Description
$\overline{CS}$	1	Input	Chip Select	An active low chip select for the serial MRAM. When chip select is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z. Multiple serial memories can share a common set of data pins by using a unique chip select for each memory.
SO	2	Output	Serial Output	The data output pin is driven during a read operation and remains Hi-Z at all other times. SO is Hi-Z when HOLD is low. Data transitions on the data output occur on the falling edge of SCK.
$\overline{WP}$	3	Input	Write Protect	A low on the write protect input prevents write operations to the Status Register.
V_{SS}	4	Supply	Ground	Power supply ground pin.
SI	5	Input	Serial Input	All data is input to the device through this pin. This pin is sampled on the rising edge of SCK and ignored at other times. SI can be tied to SO to create a single bidirectional data bus if desired.
SCK	6	Input	Serial Clock	Synchronizes the operation of the MRAM. The clock can operate up to 40 MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high. Memory operation is static so the clock can be stopped at any time.
$\overline{HOLD}$	7	Input	Hold	A low on the Hold pin interrupts a memory operation for another task. When HOLD is low, the current operation is suspended. The device will ignore transitions on the $\overline{CS}$ and SCK when HOLD is low. All transitions of HOLD must occur while $\overline{CS}$ is low.
V_{DD}	8	Supply	Power Supply	Power supply voltage from +2.7 to +3.6 volts.

2. SPI COMMUNICATIONS PROTOCOL

MR25H256 can be operated in either SPI Mode 0 (CPOL=0, CPHA =0) or SPI Mode 3 (CPOL=1, CPHA=1). For both modes, inputs are captured on the rising edge of the clock and data outputs occur on the falling edge of the clock. When not conveying data, SCK remains low for Mode 0; while in Mode 3, SCK is high. The memory determines the mode of operation (Mode 0 or Mode 3) based upon the state of the SCK when $\overline{CS}$ falls.

All memory transactions start when $\overline{CS}$ is brought low to the memory. The first byte is a command code. Depending upon the command, subsequent bytes of address are input. Data is either input or output. There is only one command performed per $\overline{CS}$ active period. $\overline{CS}$ must go inactive before another command can be accepted. To ensure proper part operation according to specifications, it is necessary to terminate each access by raising $\overline{CS}$ at the end of a byte (a multiple of 8 clock cycles from $\overline{CS}$ dropping) to avoid partial or aborted accesses.

Table 2.1 Command Codes

Instruction	Description	Binary Code	Hex Code	Address Bytes	Data Bytes
WREN	Write Enable	0000 0110	06h	0	0
WRDI	Write Disable	0000 0100	04h	0	0
RDSR	Read Status Register	0000 0101	05h	0	1
WRSR	Write Status Register	0000 0001	01h	0	1
READ	Read Data Bytes	0000 0011	03h	2	1 to ∞
WRITE	Write Data Bytes	0000 0010	02h	2	1 to ∞
SLEEP	Enter Sleep Mode	1011 1001	B9h	0	0
WAKE	Exit Sleep Mode	1010 1011	ABh	0	0

Status Register and Block Write Protection

The status register consists of the 8 bits listed in table 2.2. Status register bits BP0 and BP1 define the memory block arrays that are protected as described in table 2.3. The Status Register Write Disable bit (SRWD) is used in conjunction with bit 1 (WEL) and the Write Protection pin ($\overline{WP}$) as shown in table 2.4 to enable writes to status register bits. The fast writing speed of MR25H256 does not require write status bits. The state of bits 6,5,4, and 0 can be user modified and do not affect memory operation. All bits in the status register are pre-set from the factory to the "0" state.

Table 2.2 Status Register Bit Assignments

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRWD	Don't Care	Don't Care	Don't Care	BP1	BP0	WEL	Don't Care

Table 2.3 Block Memory Write Protection

| Status Register | | Memory Contents | |
BP1	BP0	Protected Area	Unprotected Area
0	0	None	All Memory
0	1	Upper Quarter	Lower Three-Quarters
1	0	Upper Half	Lower Half
1	1	All	None

Table 2.4 Memory Protection Modes

WEL	SRWD	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Writable	Writable
1	1	Low	Protected	Writable	Protected
1	1	High	Protected	Writable	Writable

When WEL is reset to 0, writes to all blocks and the status register are protected. When WEL is set to 1, BP0 and BP1 determine which memory blocks are protected. While SRWD is reset to 0 and WEL is set to 1, status register bits BP0 and BP1 can be modified. Once SRWD is set to 1, $\overline{WP}$ must be high to modify SRWD, BP0 and BP1.

Read Status Register (RDSR)

The Read Status Register (RDSR) command allows the Status Register to be read. The Status Register can be read at any time to check the status of write enable latch bit, status register write protect bit, and block write protect bits. For MR25H256, the write in progress bit (bit 0) is not written by the memory because there is no write delay. The RDSR command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.
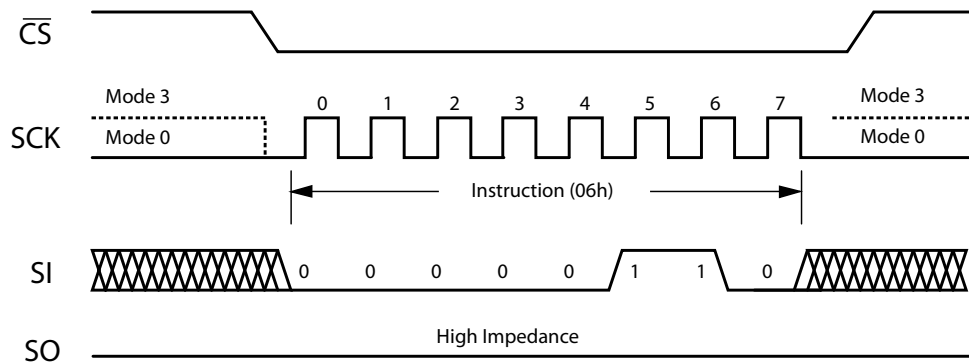
Figure 2.1 RDSR
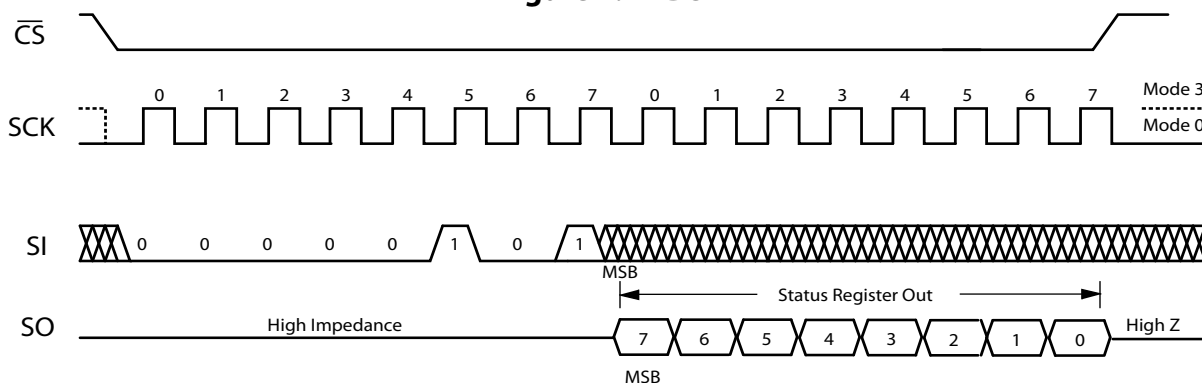
Write Enable (WREN)

The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit in the status register to 1. The WEL bit must be set prior to writing in the status register or the memory. The WREN command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.
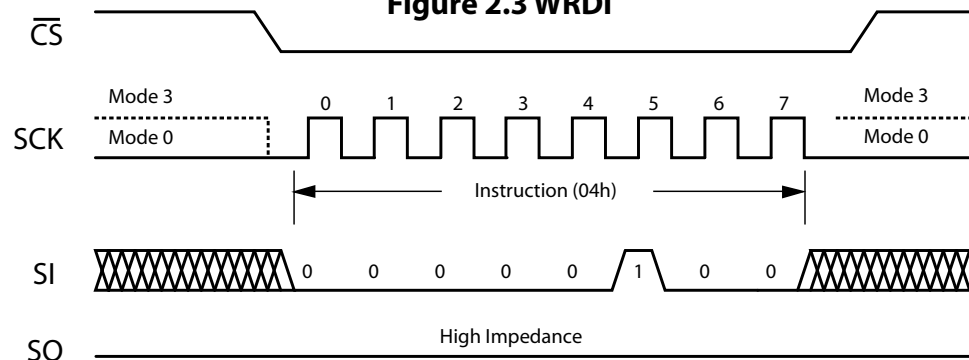
Figure 2.2 WREN

Write Disable (WRDI)

The Write Disable (WRDI) command resets the WEL bit in the status register to 0. This prevents writes to status register or memory. The WRDI command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

The WEL bit is reset to 0 on power-up or completion of WRDI.

Figure 2.3 WRDI

Write Status Register (WRSR)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. The WRSR command is not executed unless the Write Enable Latch (WEL) has been set to 1 by executing a WREN command while pin $\overline{WP}$ and bit SRWD correspond to values that make the status register writable as seen in table 2.4. Status Register bits are non-volatile with the exception of the WEL which is reset to 0 upon power cycling.

The WRSR command is entered by driving $\overline{CS}$ low, sending the command code and status register write data byte, and then driving $\overline{CS}$ high.
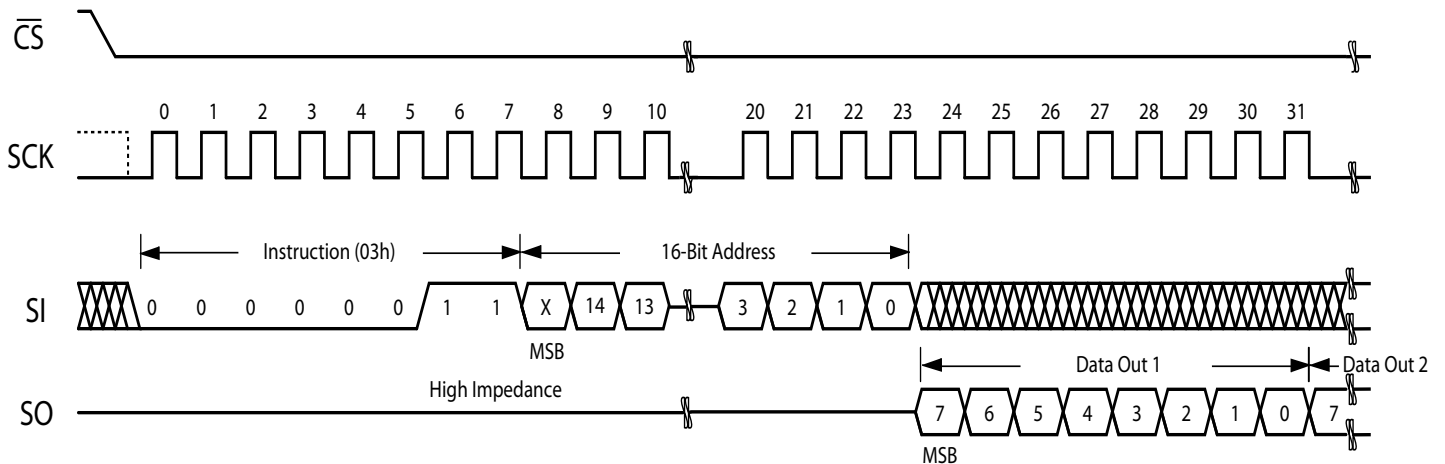
Figure 2.4 WRSR
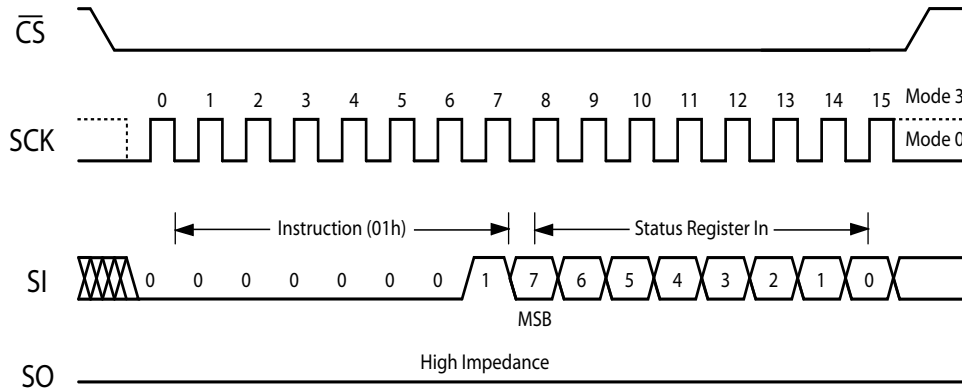
Read Data Bytes (READ)

The Read Data Bytes (READ) command allows data bytes to be read starting at an address specified by the 16-bit address. Only address bits 0-14 are decoded by the memory. The data bytes are read out sequentially from memory until the read operation is terminated by bringing $\overline{CS}$ high The entire memory can be read in a single command. The address counter will roll over to 0000h when the address reaches the top of memory.

The READ command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the SO pin. Reads continue as long as the memory is clocked. The command is terminated by bring $\overline{CS}$ high.

Figure 2.5 READ

Write Data Bytes (WRITE)

The Write Data Bytes (WRITE) command allows data bytes to be written starting at an address specified by the 16-bit address. Only address bits 0-14 are decoded by the memory. The data bytes are written sequentially in memory until the write operation is terminated by bringing $\overline{CS}$ high. The entire memory can be written in a single command. The address counter will roll over to 0000h when the address reaches the top of memory.

Unlike EEPROM or Flash Memory, MRAM can write data bytes continuously at its maximum rated clock speed without write delays or data polling. Back to back WRITE commands to any random location in memory can be executed without write delay. MRAM is a random access memory rather than a page, sector, or block organized memory making it ideal for both program and data storage.

The WRITE command is entered by driving $\overline{CS}$ low, sending the command code, and then sequential write data bytes. Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

Figure 2.6 WRITE
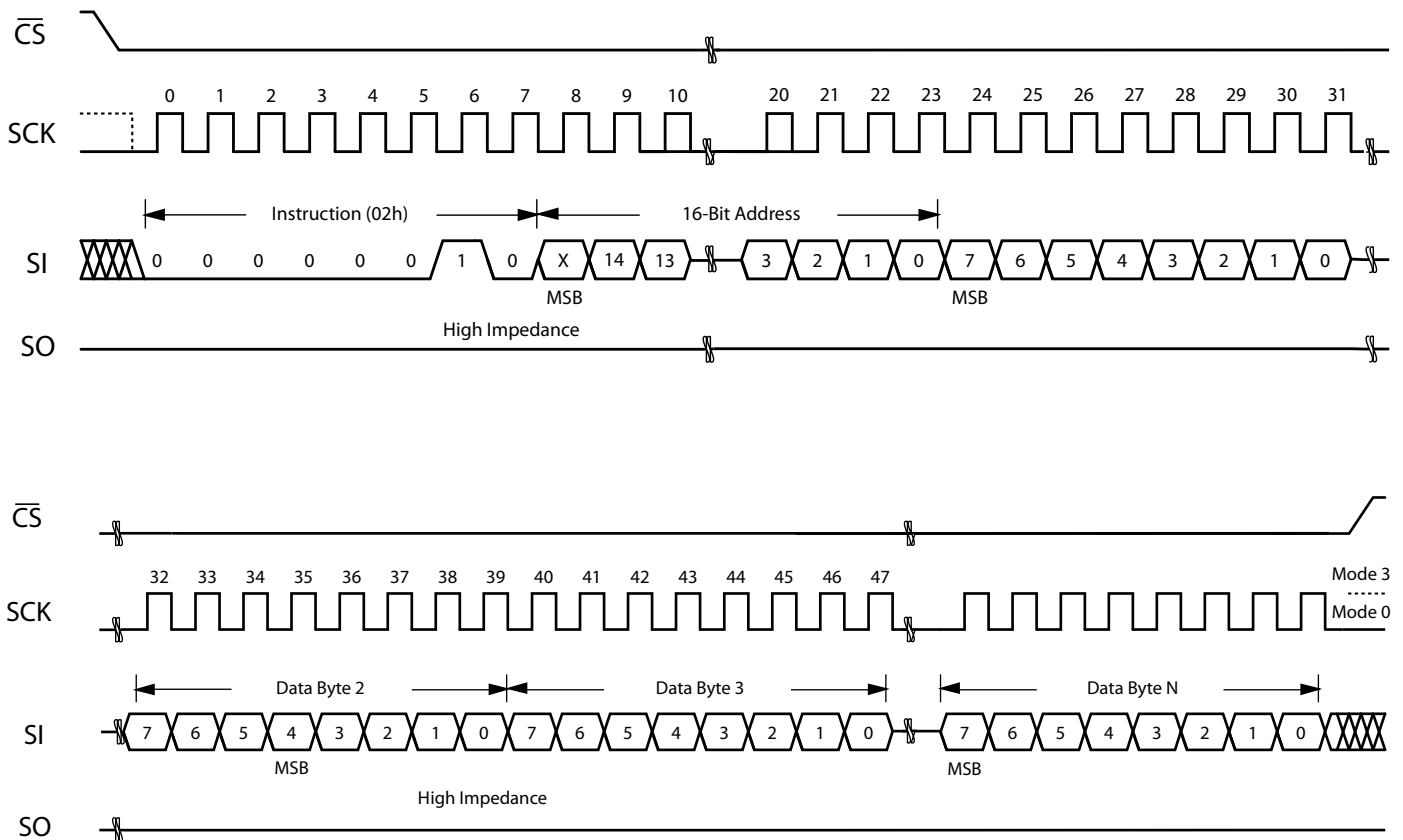
Enter Sleep Mode (SLEEP)

The Enter Sleep Mode (SLEEP) command turns off all MRAM power regulators in order to reduce the overall chip standby power to 3 µA typical. The SLEEP command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The standby current is achieved after time, t_{DP}. If power is removed when the part is in sleep mode, upon power restoration, the part enters normal standby. The only valid command following SLEEP mode entry is a WAKE command.

Figure 2.7 SLEEP
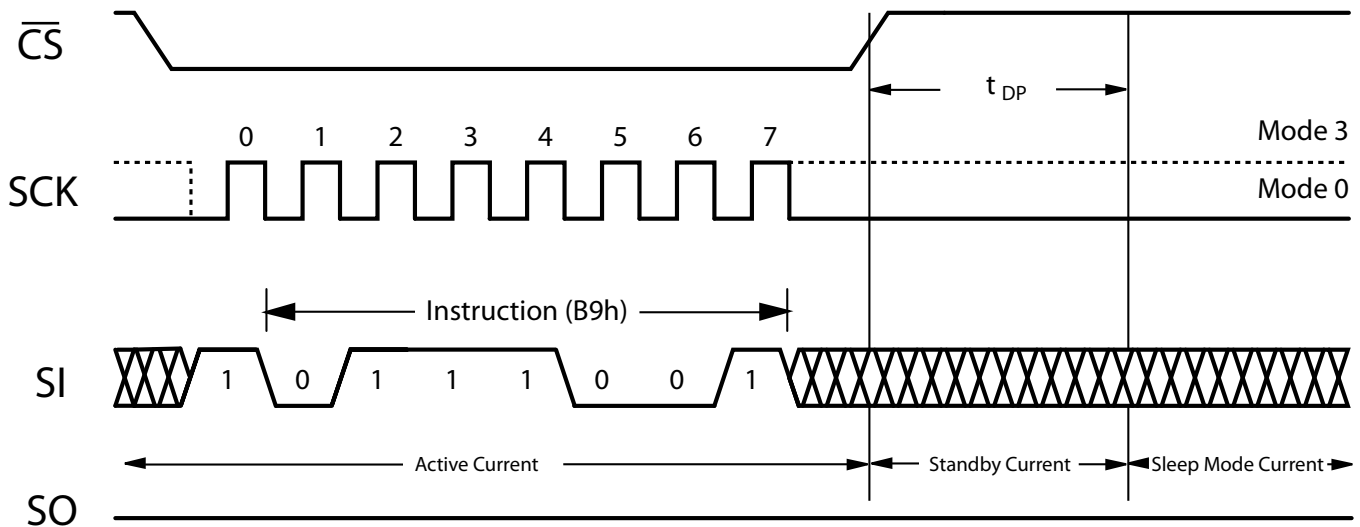
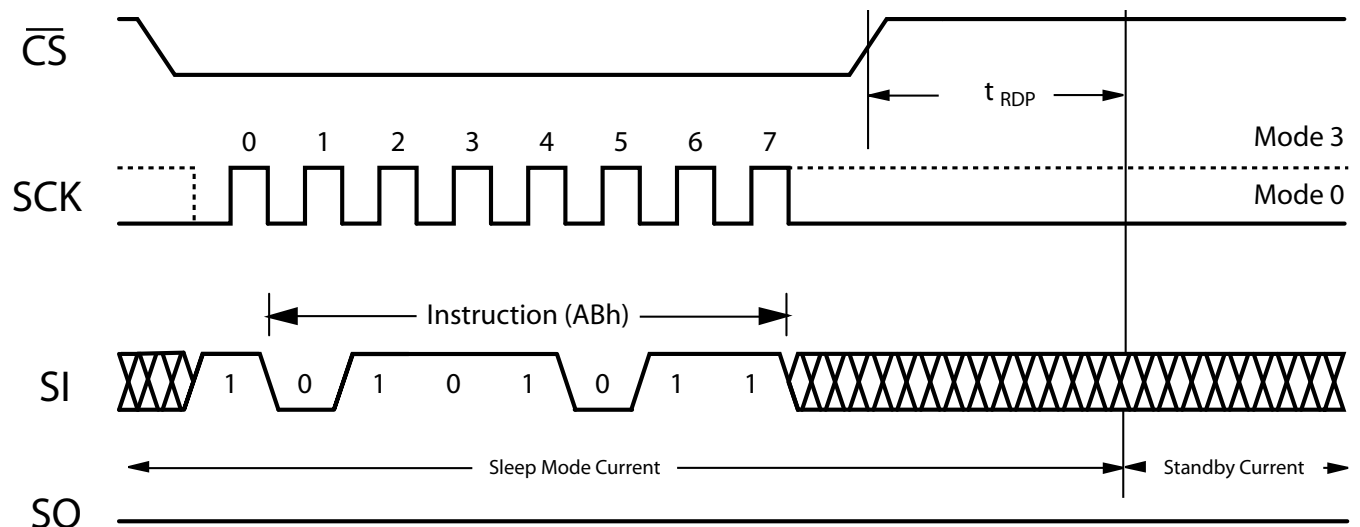## Exit Sleep Mode (WAKE)

The Exit Sleep Mode (WAKE) command turns on internal MRAM power regulators to allow normal operation. The WAKE command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The memory returns to standby mode after t_{RDP}. The $\overline{CS}$ pin must remain high until the t_{RDP} period is over.

Figure 2.8 WAKE

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the field intensity specified in the maximum ratings.

Table 3.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Supply voltage[2]	V_{DD}	-0.5 to 4.0	V
Voltage on any pin[2]	V_{IN}	-0.5 to V_{DD} + 0.5	V
Output current per pin	I_{OUT}	±20	mA
Package power dissipation	P_D	0.600	W
Temperature under bias MR25H256C (Industrial)	T_{BIAS}	-45 to 95	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write	H_{max_write}	12,000	A/m
Maximum magnetic field during read or standby	H_{max_read}	12,000	A/m

[1] Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

[2] All voltages are referenced to V_{SS}. The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.

[3] Power dissipation capability depends on package characteristics and use environment.

Table 3.2 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	V_{DD}	2.7		3.6	V
Input high voltage	V_{IH}	2.2	-	V_{DD} + 0.3	V
Input low voltage	V_{IL}	-0.5	-	0.8	V
Temperature under bias MR25H256C (Industrial)	T_A	-40	-	85	°C

Table 3.3 DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	I_{LI}	-	-	±1	µA
Output leakage current	I_{LO}	-	-	±1	µA
Output low voltage (I_{OL} = +4 mA) (I_{OL} = +100 µA)	V_{OL}	-	-	0.4 V_{DD} + 0.2	V
Output high voltage (I_{OH} = -4 mA) (I_{OH} = -100 µA)	V_{OH}	2.4 V_{DD} - 0.2	-	-	V

Table 3.4 Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
Active Read Current (@ 1 MHz)	I_{DDR}	2.5	3	mA
Active Read Current (@ 40 MHz)	I_{DDR}	5	10	mA
Active Write Current (@ 1 MHz)	I_{DDW}	6.5	13	mA
Active Write Current (@ 40 MHz)	I_{DDW}	12	27	mA
Standby Current ($\overline{CS}$ High)[1]	I_{SB}	90	115	µA
Standby Sleep Mode Current ($\overline{CS}$ High)	I_{ZZ}	3	30	µA

[1] I_{SB} current is specified with CS high and the SPI bus inactive.

4. TIMING SPECIFICATIONS

Table 4.1 Capacitance[1]

Parameter	Symbol	Typical	Max	Unit
Control input capacitance	C_{In}	-	6	pF
Input/Output capacitance	$C_{I/O}$	-	8	pF

[1] f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 4.2 AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 4.1	
Output load for all other timing parameters	See Figure 4.2	

Figure 4.1 Output Load for Impedance Parameter Measurements
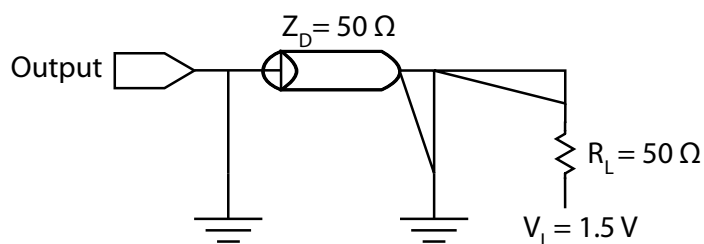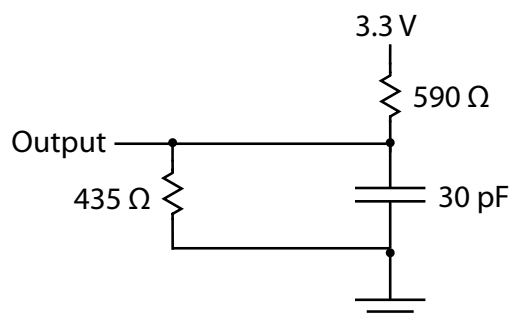

Figure 4.2 Output Load for all Other Parameter Measurements

Power-Up Timing

The MR25H256 is not accessible for a start-up time, t_{PU} = 400 μs after power up. Users must wait this time from the time when V_{DD} (min) is reached until the first $\overline{CS}$ low to allow internal voltage references to become stable. The $\overline{CS}$ signal should be pulled up to V_{DD} so that the signal tracks the power supply during power-up sequence.

Table 4.3 Power-Up

Parameter	Symbol	Min	Typical	Max	Unit
Write Inhibit Voltage	V_{WI}	2.2	-	2.7	V
Startup Time	t_{PU}	-	-	400	μs

Figure 4.3 Power-Up Timing

Ramsun International Limited   Http://www.sramsun.com
Tel:+86-755-6111 9155   E-mail: sales@sramsun.com
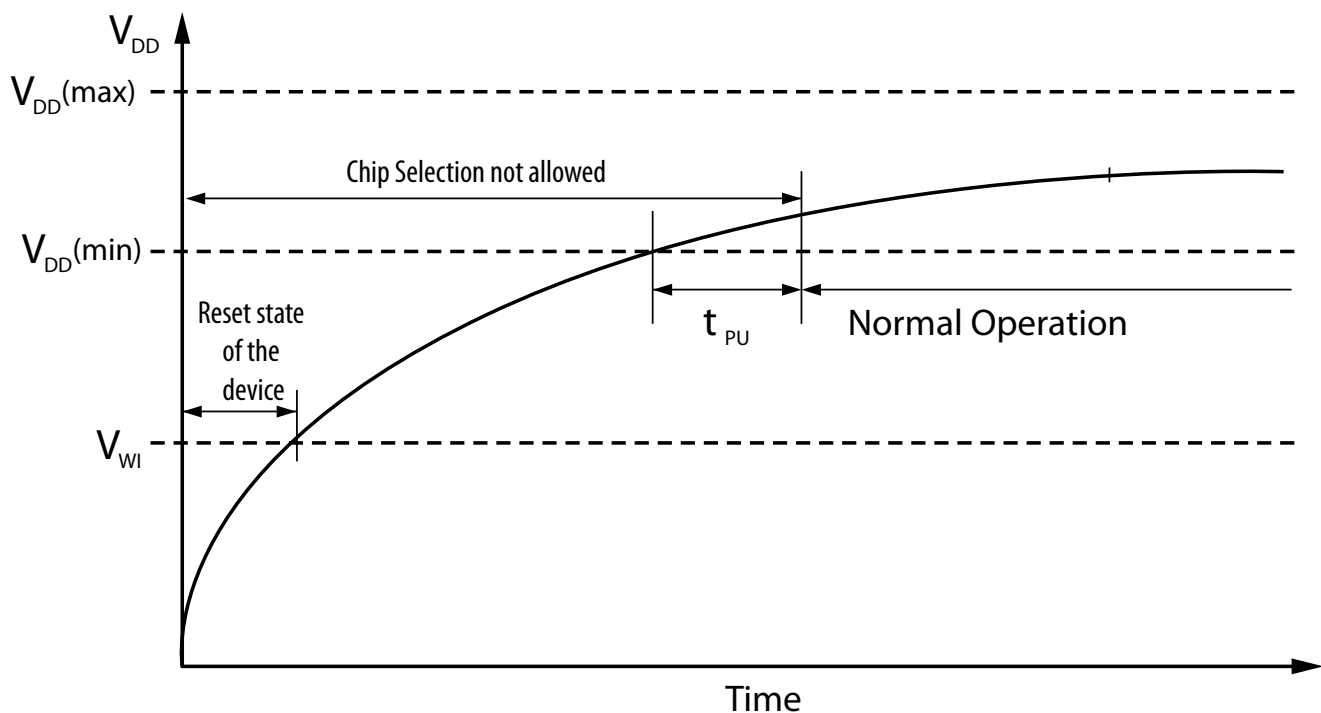
Synchronous Data Timing

Table 4.4 AC Timing Parameters[1]

Parameter	Symbol	Min	Typical	Max	Unit
SCK Clock Frequency	f_{SCK}	0	-	40	MHz
Input Rise Time	t_{RI}	-	-	50	ns
Input Fall Time	t_{RF}	-	-	50	ns
SCK High Time	t_{WH}	11	-	-	ns
SCK Low Time	t_{WL}	11	-	-	ns
Synchronous Data Timing (See figure 4.4)					
$\overline{CS}$ High Time	t_{CS}	40	-	-	ns
$\overline{CS}$ Setup Time	t_{CSS}	10	-	-	ns
$\overline{CS}$ Hold Time	t_{CSH}	10	-	-	ns
Data In Setup Time	t_{SU}	5	-	-	ns
Data In Hold Time	t_{H}	5	-	-	ns
Output Valid[2]	t_{V}	0	-	9	ns
Output Hold Time	t_{HO}	0	-	-	ns
$\overline{HOLD}$ Timing (See figure 4.5)					
$\overline{HOLD}$ Setup Time	t_{HD}	10	-	-	ns
$\overline{HOLD}$ Hold Time	t_{CD}	10	-	-	ns
$\overline{HOLD}$ to Output Low Impedance	t_{LZ}	-	-	20	ns
$\overline{HOLD}$ to Output High Impedance	t_{HZ}	-	-	20	ns
Other Timing Specifications					
$\overline{WP}$ Setup To $\overline{CS}$	t_{WPS}	5	-	-	ns
$\overline{WP}$ Hold From $\overline{CS}$	t_{WPH}	5	-	-	ns
Sleep Mode Entry Time	t_{DP}	3	-	-	µs
Sleep Mode Exit Time	t_{RDP}	400	-	-	µs
Output Disable Time	t_{DIS}	12	-	-	ns

[1] Operating Temperature Range, V_{DD}=2.7 to 3.6 V, C_L = 30 pF

Figure 4.4 Synchronous Data Timing
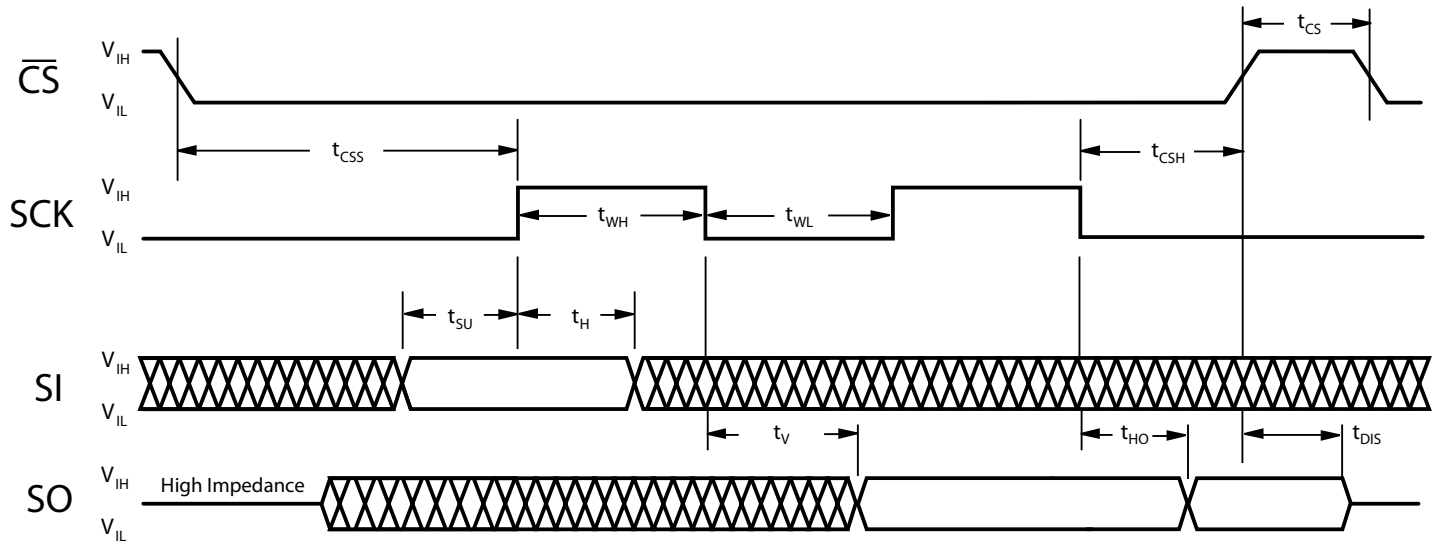
Figure 4.5 $\overline{\text{HOLD}}$ Timing
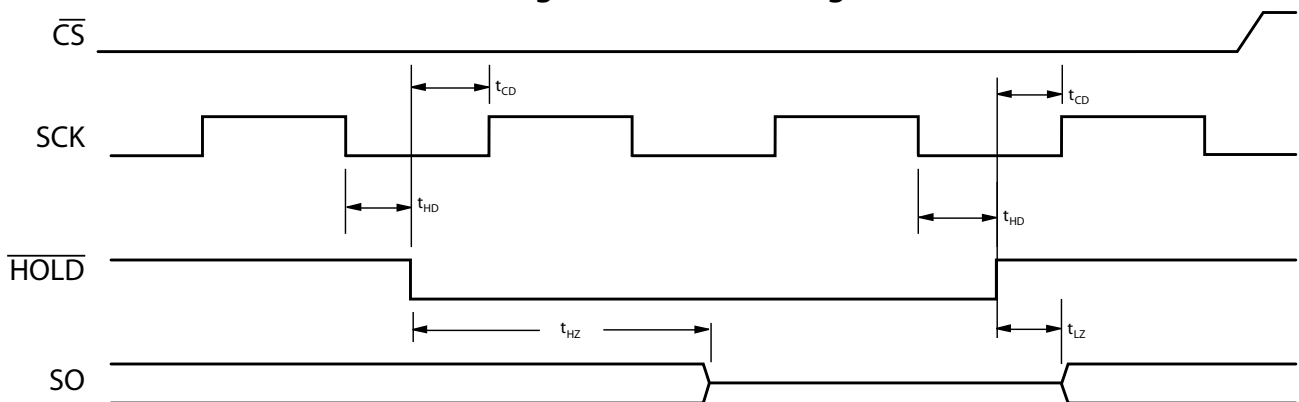
5. ORDERING INFORMATION

Figure 5.1 Part Numbering System

MR	25H	256	C	DC

Package Options

DC 8 Pin DFN on Tray

DCR 8 Pin DFN on Tape and Reel

Temperature Range

C Industrial (-40 to +85 °C ambient)

Memory Density

256 256Kb

Interface

25H High Speed Serial SPI Family

Product Type

MR Magnetoresistive RAM
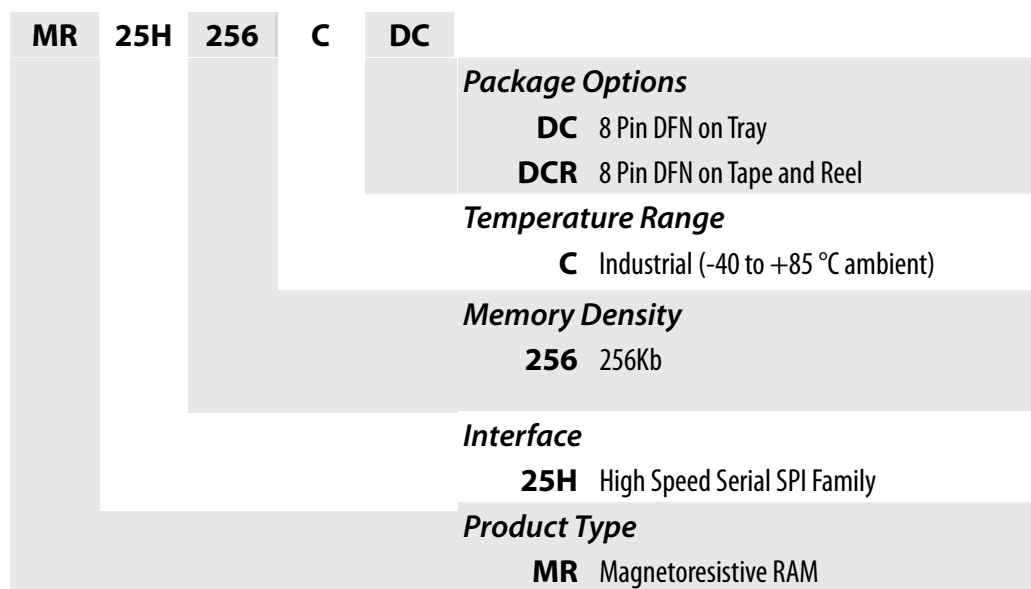
Table 5.1 Available Parts

Part Number	Description	Temperature
MR25H256CDC	3 V 256Kb Serial MRAM 8-DFN	Industrial
MR25H256CDCR	3 V 256Kb Serial MRAM 8-DFN Tape and Reel	Industrial

6. MECHANICAL DRAWINGS

Figure 6.1 DFN Package

Exposed metal Pad. Do not connect anything except V_{SS}

NOTE:

1. All dimensions are in mm. Angles in degrees.

2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08 mm.

3. Warpage shall not exceed 0.10 mm.

4. Refer to JEDEC MO-229