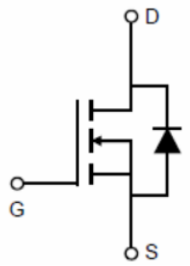
N-Channel Enhancement Mode Power MOSFET

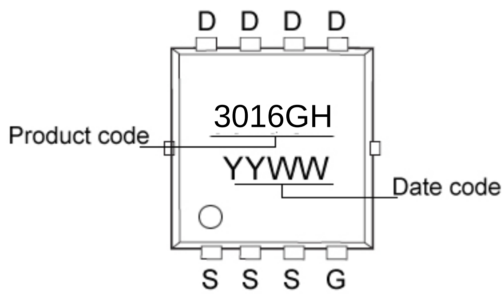
General Description

The PED3016GH is the highest performance trench N-Channel MOSFET with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

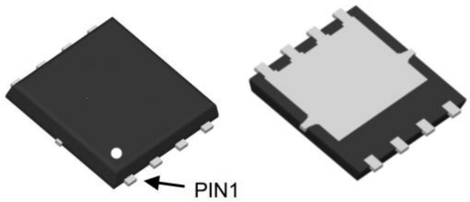
The PED3016GH meet the RoHS and Green Product requirement with full function reliability approved.



Schematic Diagram



Marking Description & Pin Assignment



DFN5X6-U-8L top&bottom view

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25˚C	Continuous Drain Current, V_{GS} @ 10V[1,7]	160	A
I_D@T_C=100˚C	Continuous Drain Current, V_{GS} @ 10V[1,7]	100	A
I_D@T_A=25˚C	Continuous Drain Current, V_{GS} @ 10V[1]	30	A
I_D@T_A=70˚C	Continuous Drain Current, V_{GS} @ 10V[1]	24	A
I_{DM}	Pulsed Drain Current[2]	310	A
EAS	Single Pulse Avalanche Energy[3]	270.1	mJ
I_{AS}	Avalanche Current	73.5	A
P_D@T_C=25˚C	Total Power Dissipation[4]	62.5	W
P_D@T_A=25˚C	Total Power Dissipation[4]	2.1	W
T_{STG}	Storage Temperature Range	-55 to 150	˚C
T_J	Operating Junction Temperature Range	-55 to 150	˚C

Thermal Data

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Symbol	Parameter	Typ.	Max.	Unit
$R_{θJA}$	Thermal Resistance Junction-Ambient[1]	---	59.5	˚C/W
$R_{θJC}$	Thermal Resistance Junction-Case[1]	---	2	˚C/W

Electrical Characteristics (T =25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T$	BVDSS Temperature Coefficient	Reference to 25˚C , I_D=1mA	---	0.008	---	V/˚C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=30A	---	1.2	1.5	mΩ
		V_{GS}=4.5V , I_D=15A	---	1.9	2.5	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	---	2.5	V
$\triangle V_{GS(th)}$	$_{GS(th)}$ Temperature Coefficient		---	-5.3	---	mV/˚C
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V , T_J=25˚C	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55˚C	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=15A	---	62	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	0.8	---	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=15V , V_{GS}=10V , I_D=15A	---	51	---	nC
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=15A	---	24	---	
Q_{gs}	Gate-Source Charge		---	7.6	---	
Q_{gd}	Gate-Drain Charge		---	10.3	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3.3Ω I_D=15A	---	12.1	---	ns
T_r	Rise Time		---	43.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	37.1	---	
T_f	Fall Time		---	9.0	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	3100	---	pF
C_{oss}	Output Capacitance		---	1960	---	
C_{rss}	Reverse Transfer Capacitance		---	69	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.1mH , I_{AS}= 42.1A	88.62	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	160	A
I_{SM}	Pulsed Source Current[2,6]		---	---	310	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25˚C	---	---	1.2	V
trr	Reverse Recovery Time	IF=15A , dI/dt=100A/µs , T_J=25˚C	---	159	---	nS
Qrr	Reverse Recovery Charge		---	194	---	nC

Note :

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH

4.The power dissipation is limited by 150˚C junction temperature

5.The Min. value is 100% EAS tested guarantee.

6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

7.The maximum current rating is package limited.

Typical Characteristics

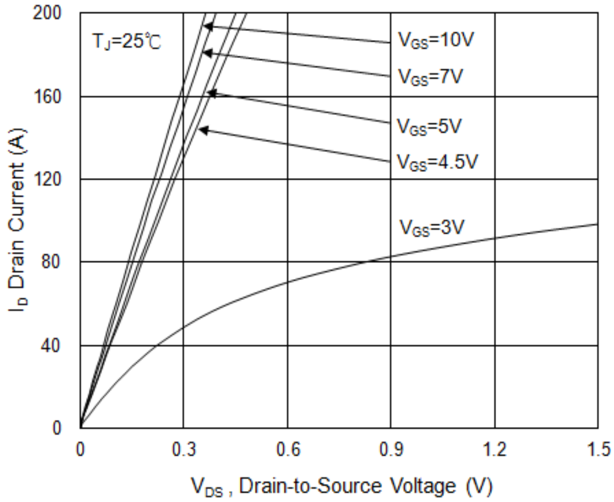


Fig.1 Typical Output Characteristics

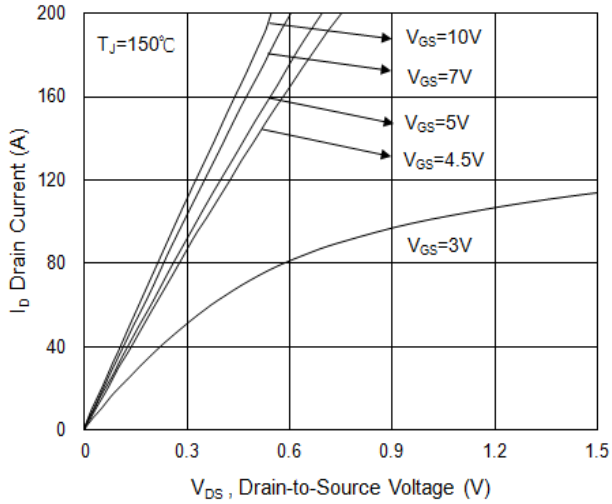


Fig.2 Typical Output Characteristics

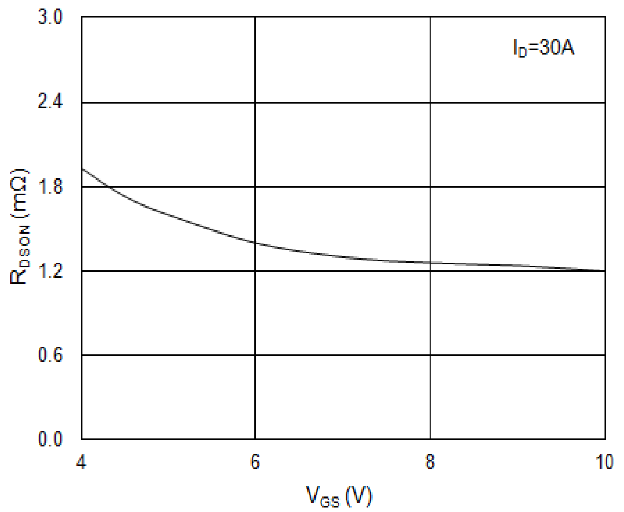


Fig.3 On-Resistance vs. Gate-Source

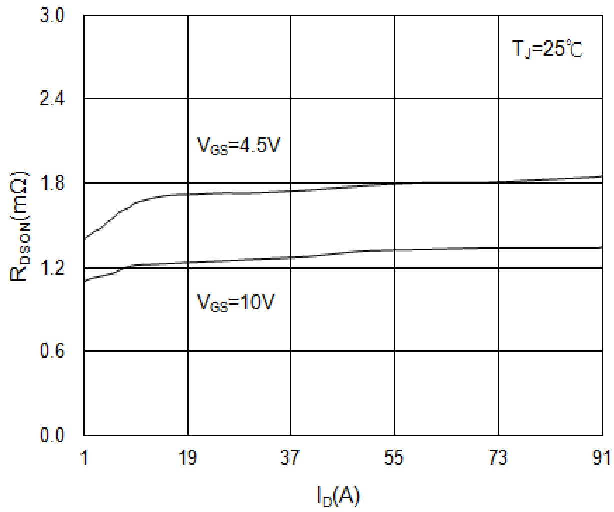


Fig.4 Drain-Source On-State Resistance

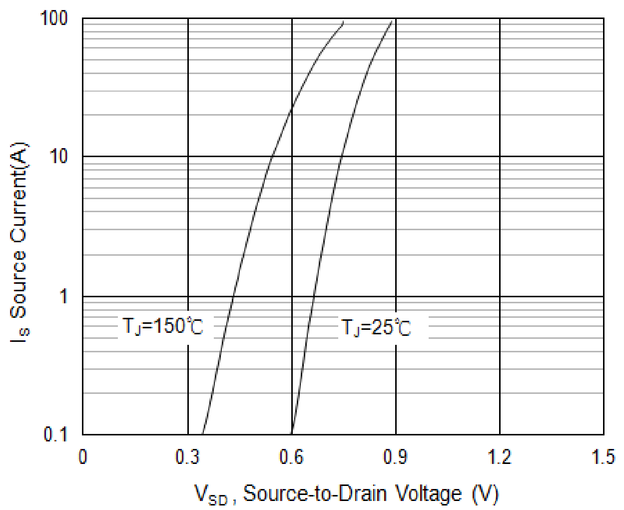


Fig.5 Forward Characteristics of Reverse

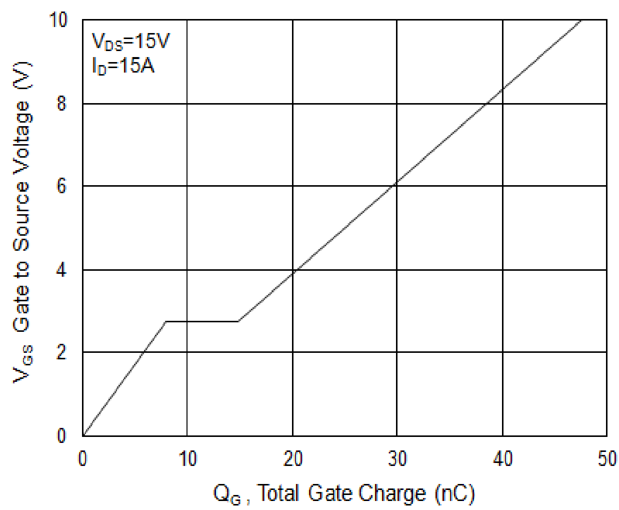


Fig.6 Gate-Charge Characteristics

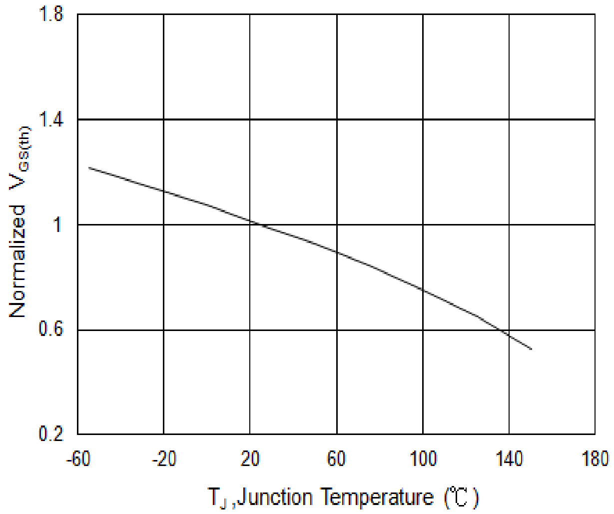


Fig.7 Normalized $V_{GS(th)}$ vs. T_J

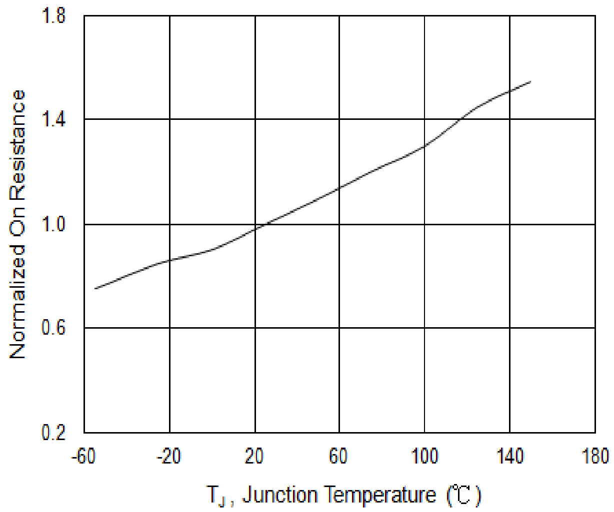


Fig.8 Normalized R_{DSON} vs. T_J

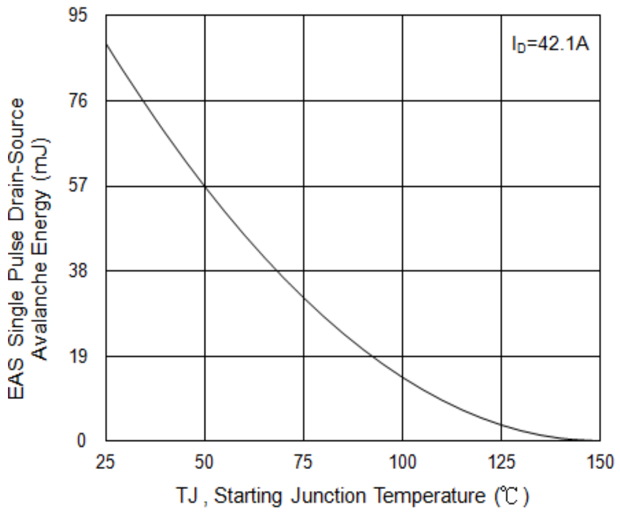


Fig.9 Single Pulse Avalanche Energy

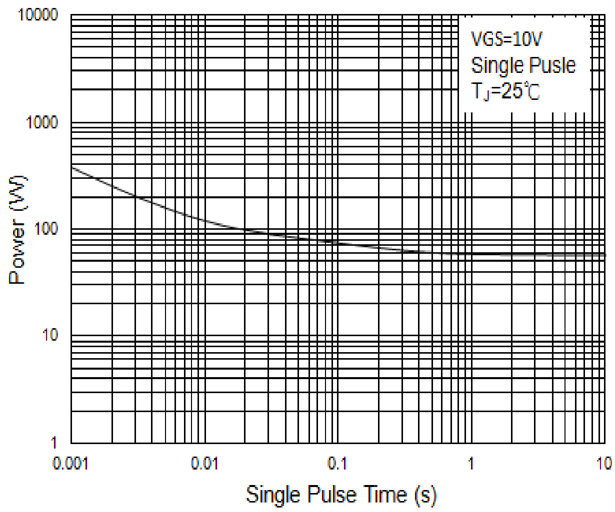


Fig.10 Single Pulse Maximum Power Dissipation

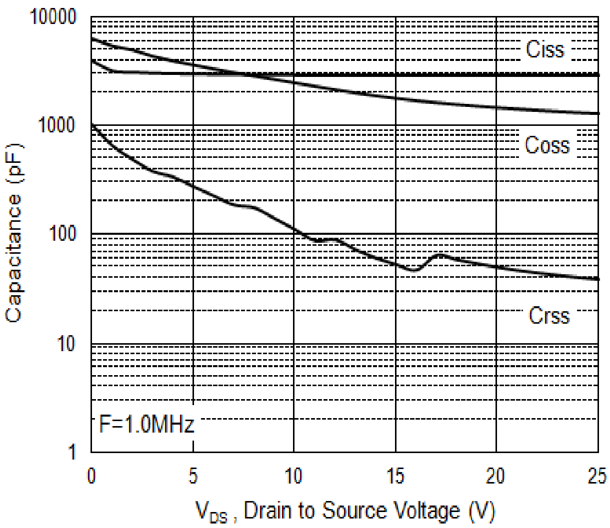


Fig.11 Capacitance

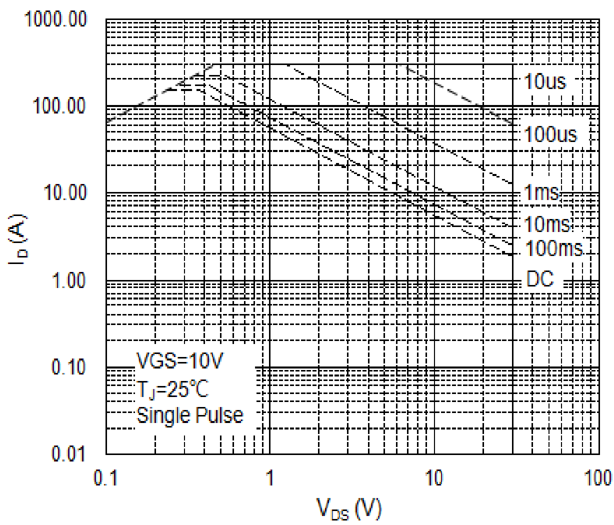


Fig.12 Safe Operating Area

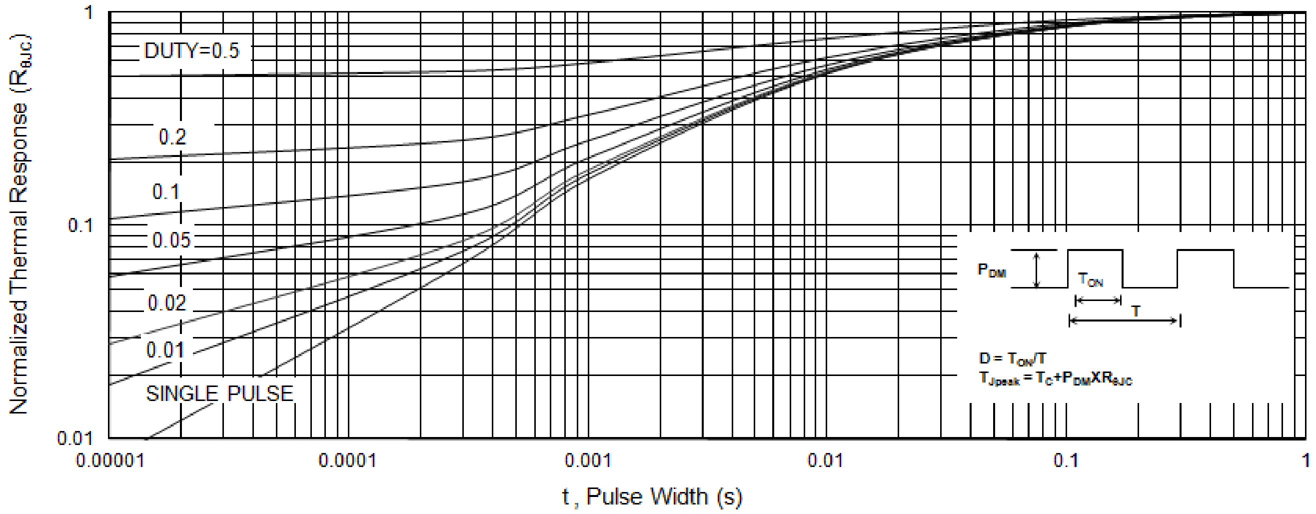
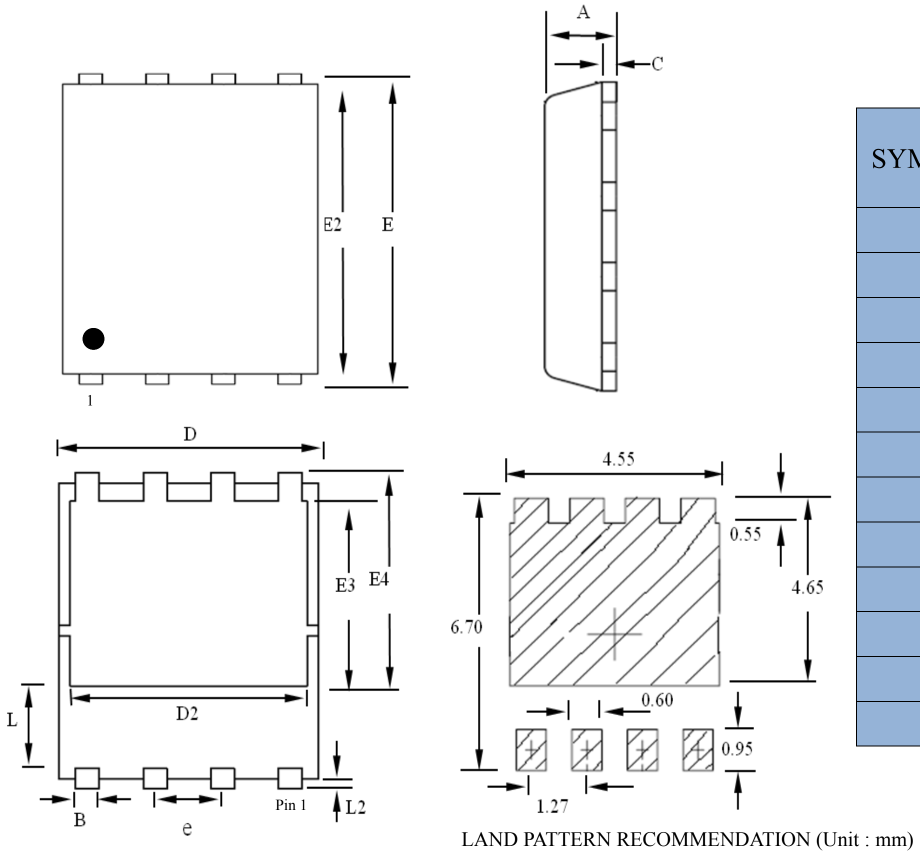


Fig.13 Transient Thermal Impedance

DFN5X6-U-8L Package Information



LAND PATTERN RECOMMENDATION (Unit : mm)

SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.00	1.20
B	0.33	--	0.51
C	0.20	--	0.34
D	4.98	--	5.20
D2	3.60	--	4.22
E	5.90	--	6.13
E2	5.50	--	5.84
E3	3.18	--	4.30
E4	3.69	--	4.39
L	1.10	--	1.39
L2	0.02	--	0.33
e	--	1.27	--

Note:
1. ALL DIMENSIONS LISTED ON THE DRAWING MEETING JEDEC STANDARD.
2. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
3. RECOMMENDED LAND PATTERN DESIGN IS ONLY FOR REFERENCE