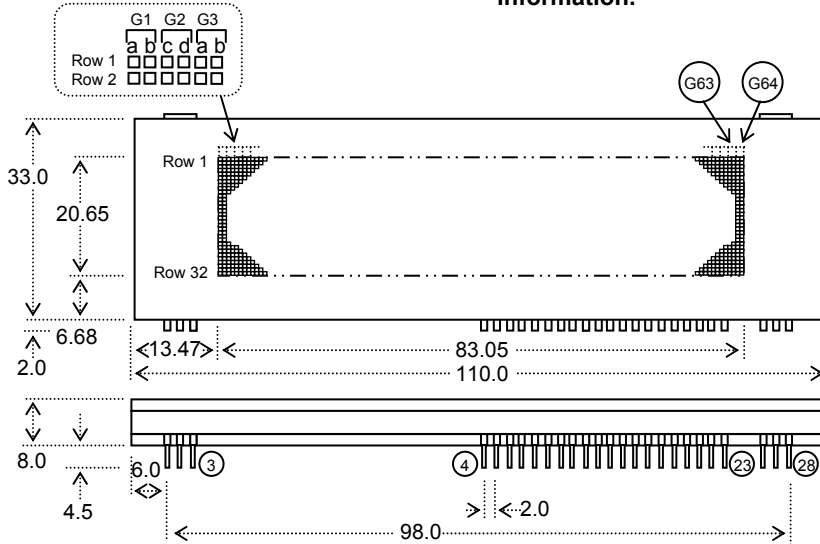


# Graphic Dot Matrix Chip In Glass VFD

# MN12832JC

- ❑ 128 x 32 Graphic Dot Matrix
- ❑ Chip in Glass Driver IC
- ❑ High Brightness Blue Green Display
- ❑ Synchronous Serial Interface
- ❑ Low Pinout Count
- ❑ Wide Operating Temperature

This VF glass includes 3 x 64 bit serial shift register, latched drivers which connect to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor. The a.c. filament supply (F1, F2) can be derived from a source of 50Hz to 60Hz. Consult our application notes for further information.



### PIN OUT

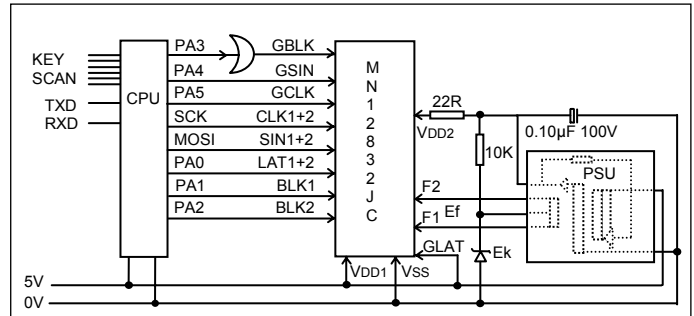
Pin	Sig	Pin	Sig
1	F1	14	GBLK
2	F1	15	GLAT
3	F1	16	GCLK
4	BLK1	17	GSIN
5	LAT1	18	GSOUT
6	CLK1	19	NC
7	SIN1	20	SIN2
8	NC	21	CLK2
9	VDD2	22	LAT2
10	VDD2	23	BLK2
11	VSS	26	F2
12	VSS	27	F2
13	VDD1	28	F2

Dimensions in mm. See full spec for tolerances

### ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	VDD1	4.5	5.0	5.5	V	VSS=0V
Logic Current	I <sub>DD1</sub>	-	3.0	6.0	mA	VDD1=5V
Filament Voltage	E <sub>f</sub>	3.6	4.0	4.4	Vac	VDD2=0V
Filament Current	I <sub>f</sub>	180	200	220	mAac	VDD2=0V
Display Voltage	VDD2	50.0	60.0	63.0	V	VSS=0V
Display Current	I <sub>DD2</sub>	-	20.0	30.0	mA	VDD2=60V
Filament Bias	E <sub>k</sub>	-	5.0	-	V	VSS=0V
Logic High Input	V <sub>IH</sub>	VDD1x0.8	-	VDD1	V	VSS=0V
Logic Low Input	V <sub>IL</sub>	0	-	+0.7	V	VSS=0V
Logic High Input	I <sub>IH</sub>	-	-	5.0	µA	VDD1=5V
Logic Low Input	I <sub>IL</sub>	-400	-250	-35	µA	VDD1=5V

### INTERFACE EXAMPLE

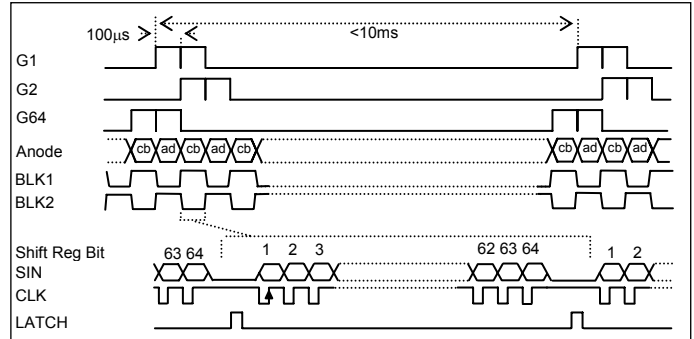


### ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Display Area (XxY mm)	83.05 x 20.65
Dot Size/Pitch (XxY mm)	0.5 x 0.5/0.65 x 0.65
Luminance	600 cd/m <sup>2</sup> Typ.
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

- The power on rise time should be less than 50ms.
- The 22R resistor at the VDD2 input is required to prevent current surge during switching.
- If scanning of the display stops with VDD2 applied, the BLK input must be set high to prevent damage to the display.

### MULTIPLEX TIMING



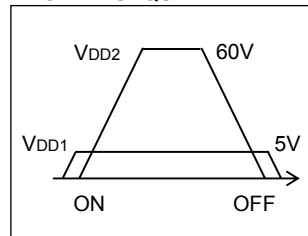
### SHIFT REGISTER ASSIGNMENT

Electrode	Bit Numbers
Grid G1-G64	GSIN1-64
Row 1 'ad'	SIN1 1,2
Row 1 'cb'	SIN2 1,2
Row 2 'ad'	SIN1 3,4
Row 2 'cb'	SIN2 3,4
...	...
Row 32 'ad'	SIN1 63,64
Row 32 'cb'	SIN2 63,64

### INTERFACE TIMING

Parameter	Time
CLK Cycle	200ns min
CLK High	80ns min
CLK Low	80ns min
SIN Setup	40ns min
SIN Hold	30ns min
LAT High	300ns min
CLK then LAT	250ns min
BLK Hold	5µs min

### POWER SEQUENCE



### CONTACT

**Noritake Sales Office Tel Nos**  
 Nagoya Japan: +81 (0)52-561-9867  
 Canada: +1-416-291-2946  
 Chicago USA: +1-847-439-9020  
 Munchen (D): +49 (0)89-3214-290  
 Itron UK: +44 (0)1493 601144  
 Rest Europe: +49 (0)61-0520-9220  
 www.noritake-itrn.com  
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