HIGH-VOLTAGE MIXED-SIGNAL IC

UC1701

64x128 STN Controller-Driver

MP Specifications
Datasheet Revision: 1.02

IC Version: e_A
April 20, 2016

ULTRACHIP

The Coolest LCD Driver, Ever!

Table of Content

UC1701

Single-Chip, Ultra-Low Power
64COM by 128SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1701e is an advanced low power consumption mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power column and row drivers, the IC contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- ESL and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver support 64x128 graphics STN LCD panels.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 4-wire (S8) and 3-wire (S9) serial interfaces.
- Ultra-low power consumption under all display patterns.
- Fully programmable Mux Rate, Bias Ratio and Frame Rate allow many flexible power management options.
- Software programmable frame rates.
- Four software programmable temperature compensation coefficients.
- 3-x internal charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- On-chip Power-ON Reset makes RSTB pin optional.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} (digital) range (Typ.): 2.0V ~ 3.3V
  $V_{DD2/3}$ (analog) range (Typ.): 2.2V ~ 3.3V
  V_{LCD} range: 2.83V ~ 5.51V
- Available in gold bump dies
- COM/SEG bump information
  Bump pitch: 24 μM
  Bump gap: 12 μM
  Bump surface: 1500 μM^2
- **Remark:** Contact UltraChip for a visual inspection document (03-DOC-093).

ORDERING INFORMATION

Part Number	MTP	I^2C	Description
UC1701eGAA	No	No	Gold Bumped Die, with Bump Height: 9uM
UC1701eGBA	No	No	Gold Bumped Die, with Bump Height: 15uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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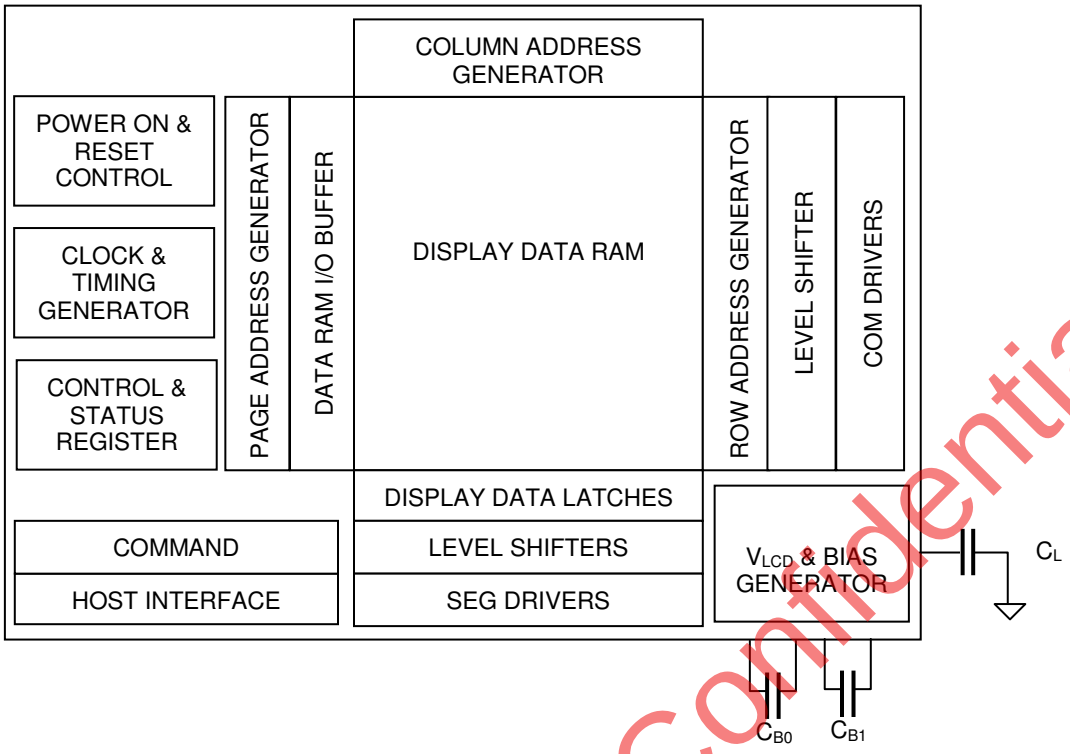
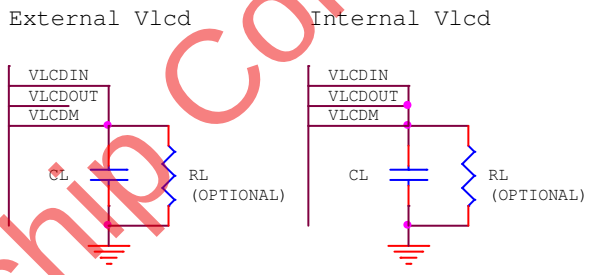
BLOCK DIAGRAM



PIN DESCRIPTION

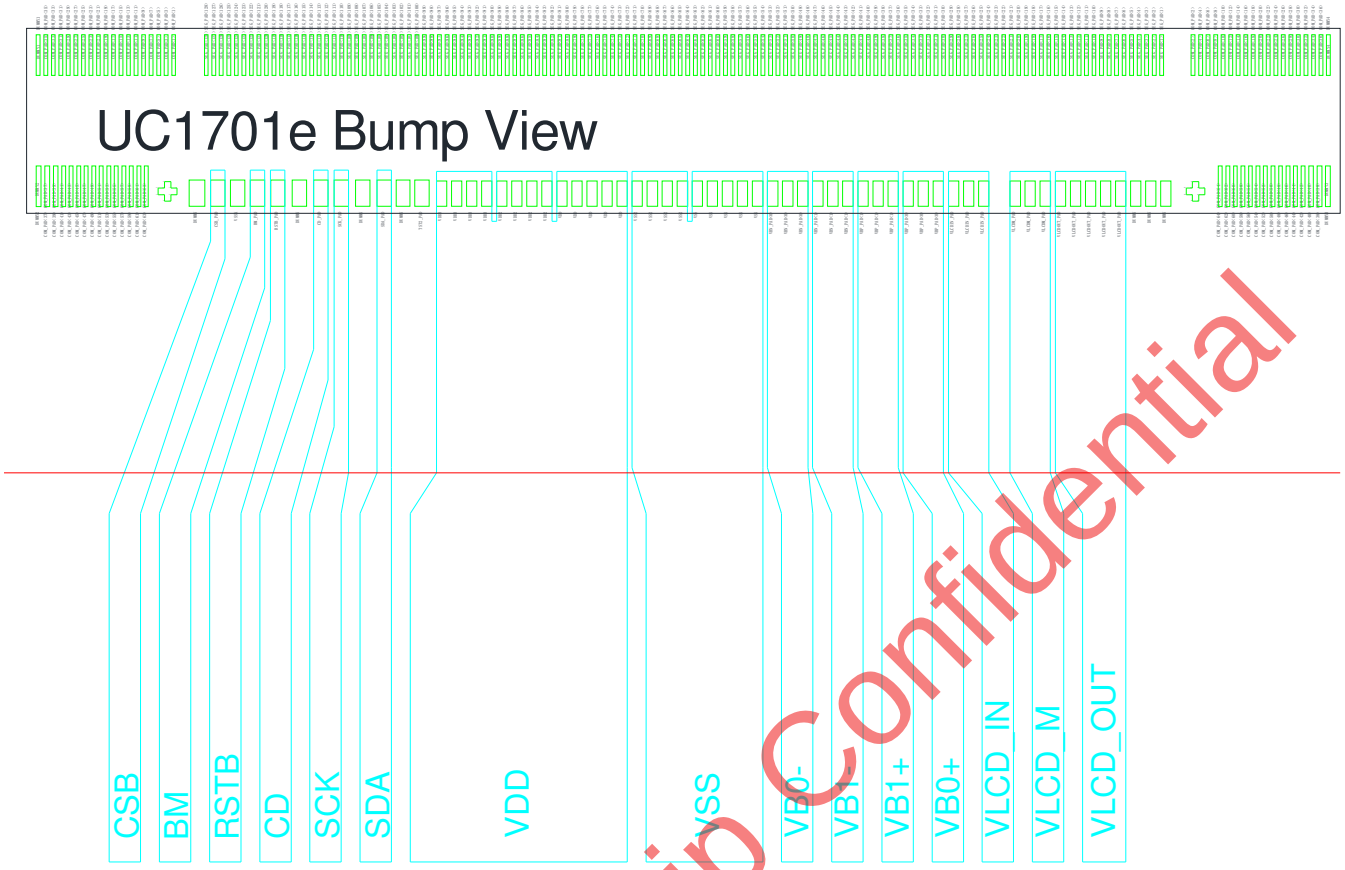
Pin Name (Pad Name)	Type	Pin Count	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	5 4 4	V_{DD} supplies for Display Data RAM and digital logic, V_{DD2} supplies for V_{LCD} and V_D generator, V_{DD3} supplies for V_{BIAS} and other analog circuits. V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.3V \geq V_{DD2/3} \geq V_{DD}$ ITO trace resistance needs to be minimized for V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	5 4	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. In COG applications, minimize the ITO resistance for both V_{SS} and V_{SS2}.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} V_{B1-} V_{B0+} V_{B0-} (VBP_PAD<1> VBN_PAD<1> VBP_PAD<0> VBN_PAD<0>)	PWR	3 3 3 3	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. See the "LCD Voltage Setting" section for more details. In COG application, the resistance of these ITO traces directly affects the SEG driving strength of the resulting LCD module. Minimize these trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT} V_{LCDM} (VLCDIN_PAD VLCDOUT_PAD VLCDM_PAD)	PWR	3 5 3	When using external, connect V_{LCDIN} and V_{LCDM} together. When using internal V_{LCD}, connect these 3 pads together.  Capacitor C_L should be connected between V_{LCD} and V_{SS}. In COG applications, keep the ITO trace resistance around 70 Ω .

Note:
- Recommended capacitor values:
  C_B: 2.2μF/5V or 300x(LCD load capacitance), whichever is higher.
  C_L: 330nF/16V is appropriate for most applications.

Pin Name (Pad Name)	Type	Pin Count	Description
HOST INTERFACE			
BM (BM_PAD)	I	1	Bus mode: The interface bus mode is determined by BM by the following relationship: BM: 0b → Mode: 4-wire SPI w/ 8-bit token (S8: conventional) BM: 1b → Mode: 3-wire SPI w/ 9-bit token (S9: conventional)
CSB (CSB_PAD)	I	1	Chip Select. Chip is selected when CSB = "L". When the chip is not selected, SDA and SCK will be of high impedance.
RSTB (RSTB_PAD)	I	1	When RST="L", all control registers are re-initialized by their default states. Since UC1701e has built-in Power-On Reset. The RSTB pin is not required for normal chip operation. An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.
CD (CD_PAD)	I	1	Select Control data or Display data for read/write operation. In S9 mode, the CD pin is not used. Connect it to V_{DD} or V_{SS} when not used. "L": Control data "H": Display data
SDA SCK (SDA_PAD SCK_PAD)	I/O	1 1	Bi-directional bus for host interfaces.
HIGH VOLTAGE LCD DRIVER OUTPUT			
COM1 ~ COM64 (COM_PAD <1>~<64>)	HV	64	COM (row) driver outputs. Support up to 64 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 64, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 64] open-circuit.
SEG1 ~ SEG128 (SEG_PAD <1>~<128>)	HV	128	SEG (column) driver outputs. Support up to 128 pixels. Leave unused SEG drivers open-circuit.
MISC. PINS			
V_{SSX}		1	Auxiliary Vss. This pin is connected to the main Vss bus within the IC to facilitate chip configurations in COG application. There's no need to connect V_{DDX} to main Vss externally and it should *NOT* be used to provide Vss power to the chip.
TST2 (TST2_PAD)	I/O	1	Test I/O pins. Leave these pins open during normal use.
Dummy, Dummy1~4		7 1x4	NC.

Note: Several control registers will specify "0 based index" for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value range for those index register will be 0~63 for COM and 0~127 for SEG.

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The operation condition, V_{DD}=2.0V (typical), should be satisfied under all operating conditions. UC1701e's peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1701e's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 1.8V and cause the IC to malfunction.

CONTROL REGISTERS

UC1701e contains registers, which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, Command Table and Command Description.

Name: The Symbolic reference of the register. Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after Power-Up-Reset and System-Reset.

Name	Bits	Default	Description
CA	7	00H	Display Data RAM Column Address. Value range is 0 ~ 127 (Used in Host for Display Data RAM access)
PA	3	0H	Display Data Page Row Address. Value range is 0 ~ 7. (Used in Host for Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b:3 01b: 4 **10b: 5** 11b: 6
TC	2	0H	Temperature Compensation (per °C) **00b: -0.00%** 01b: -0.05% 10b: -0.10% 11b: -0.15%
PM	7	6EH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PC	3	5H	Power Control. 0010 10## PC[1:0]: low pump charge current select 00b: 0.15mA **01b: 0.25mA** 10b: 0.4mA 11b: 0.5mA PC[2]: 0b: External VLCD **1b: Internal VLCD (3x charge pump)**
DC	1	0H	Display Control: DC: Display ON/OFF (Default **0: OFF**)
LC	4	2H	LCD Control: LC[1:0]: Master Clock(MCLK) freq. (MHz) 00b: 0.184 (V_{LCD} range: 2.83V ~ 4.9V) 01b: 0.524 **10b: 0.693** 11b: 1.012 LC[2]: MX, Mirror X. SEG/Column sequence inversion(Default **0b: OFF**) LC[3]: MY, Mirror Y. COM/Row sequence inversion (Default **0b: OFF**)
CKC	5	06H	Clock Control: CKC[4:0] : SCLK divider 00000b: Disable divide : SCLK freq.=MCLK 00001b~11111b: SCLK freq.=MCLK/CKC[4:0] /2
LW	7	16H	SCLK Num. per line LW > 20 ; LW>(ISOF+ISOE+10)
ISOF	3	1H	COM Isolation clock num. in the front of the line ISOF+ISOE>0
ISOE	3	0H	COM Isolation clock num. in the end of the line ISOF+ISOE>0
CEN	6	3FH	COM scanning end (last COM with full line cycle, 0-based index)
APC	8	N/A	For UltraChip only. Please do not use.
TT	8	N/A	For UltraChip only. Please do not use.
Get Status Sequence			
IC_rev, DE, MX, MY			IC version, Display Enable, Mirror X, Mirror Y

COMMAND TABLE

The following is a list of host commands supported by UC1701e

C/D : 0: Control, 1: Data W/R : 0: Write Cycle, 1: Read Cycle D7~D0 : #: Useful Data bits – : Don't Care

No.	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte (Double-byte command)	0	0	0	0	0	0	0	0	0	1	Write 1 byte	N/A
		1	0	#	#	#	#	#	#	#	#		
2	Read Data Byte (Double-byte command)	0	0	0	0	0	0	0	0	1	0	Read 1 byte	N/A
		1	1	#	#	#	#	#	#	#	#		
3	Get Status (Double-byte command)	0	0	0	0	0	0	0	0	1	1	Get Status	N/A
		1	1	IC_rev	DE	MX	MY	0	0	0	0		
4	Set Column Address (Double-byte command)	0	0	0	0	0	0	0	1	0	0	Set CA[6:0]	0
		1	0	0	#	#	#	#	#	#	#		
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	101b
7	Set Adv. Program Control (Double-byte command)	0	0	0	0	1	1	0	0	0	0	Set APC[7:0]	N/A
		1	0	#	#	#	#	#	#	#	#		
8	Set Page Address	0	0	1	0	1	1	0	#	#	#	Set PA[2:0]	0
9	Set Vbias Potentiometer (Double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[6:0]	6EH
		1	0	0	#	#	#	#	#	#	#		
10	Set LC	0	0	1	0	1	0	#	#	#	#	Set LC[3:0]	0010b
11	Set Display Enable unlock	0	0	1	1	0	0	1	0	0	1	Set DC	0b
	Set Display Enable	1	0	1	0	1	0	1	1	1	#		
12	System Reset unlock	0	0	1	1	1	0	0	0	0	1	System Reset	N/A
	Set System Reset	1	0	1	1	1	0	0	0	1	0		
13	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
14	Set Test Control (Double-byte command)	0	0	1	1	1	0	0	1	0	TT	For testing only.	N/A
		1	0	#	#	#	#	#	#	#	#	Do not use.	
15	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 5
16	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[5:0]	63
		1	0	0	0	#	#	#	#	#	#		
17	Set LW (Triple-byte command)	0	0	1	0	0	0	0	0	1	0	Set LW[6:0]	16H
		1	0	0	0	0	0	0	0	0	0		
		1	0	0	#	#	#	#	#	#	#		
18	Set ISOF (Triple-byte command)	0	0	1	0	0	0	0	0	1	0	Set ISOF[2:0]	01H
		1	0	0	0	0	0	0	0	0	1		
		1	0	0	0	0	0	0	#	#	#		
19	Set ISOE (Triple-byte command)	0	0	1	0	0	0	0	0	1	0	Set ISOE[2:0]	00H
		1	0	0	0	0	0	0	0	1	0		
		1	0	0	0	0	0	0	#	#	#		
20	Set CKC	0	0	1	0	0	0	0	0	1	1	Set CKC[4:0]	06H
		1	0	0	0	0	#	#	#	#	#		

Note: Any bit pattern other than those listed above may result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write 1 byte Data to Memory	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	8-bit data written to SRAM							

2. Read Data Byte

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read 1 byte Data from Memory	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	1	1	8-bit data read from SRAM							

Write/Read Data Byte (Command 1,2) access Display Data RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of the page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches the end of the page, CA will be reset to 0 and PA will increase or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM, PA will be wrapped around to the other end of RAM and continue.

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
	1	1	IC_rev	DE	MX	MY	**0**	**0**	**0**	**0**

IC_rev: IC version.
DE: Display Enable flag. DE=1 when display is enabled.
MX: Status of register LC[2], mirror X.
MY: Status of register LC[3], mirror Y.

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address, CA[6:0] (Double-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
	1	0	**0**	CA6	CA5	CA4	CA3	CA2	CA1	CA0

Set the SRAM column address before Write/Read memory from host interface.

CA value range: 0~127 (**Default: 00H**)

5. Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

TC[1:0]: Temperature compensation curve definition:

00b= -0.00%/ °C 01b= -0.05%/ °C 10b= -0.10%/ °C 11b= -0.15%/ °C

6. Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Power Control, PC[2:0]	0	0	**0**	**0**	**1**	**0**	**1**	PC2	PC1	PC0

PC[1:0]: to select low-pump charge current
00b: 0.15mA **01b: 0.25mA** 10b: 0.4mA 11b: 0.5mA

PC[2]: Internal / External VLCD selection
0b: External VLCD **1b: Internal VLCD (3x charge pump)**

7. Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control, APC[7:0] (Double-byte command)	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**
	1	0	APC[7:0] register parameter							

For UltraChip only. Do *NOT* use.

8. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address, PA[2:0]	0	0	**1**	**0**	**1**	**1**	**0**	PA2	PA1	PA0

Display Data Page Row Address. Value range is 0 ~ 7. (**Default: 0H**)

9. Set V_{BIAS} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer, PM [6:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	**0**	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program PM[6:0] to fine tune VBIAS and VLCD. See section `LCD Voltage Setting` for more detail.

Effective range: 0 ~ 127 (**Default: 6EH**)

10. Set LC

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Control, LC[3:0]	0	0	**1**	**0**	**1**	**0**	LC3/MY	LC2/MX	LC1	LC0

LCD Control:

LC[3]: MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image. (Default: **0b: OFF**)

LC[2]: MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data. (Default: **0b: OFF**)

LC[1:0]: Master Clock Frequency (MCLK)

00b: 0.184 MHz (VLCD range: 2.83V ~ 4.9V) 01b: 0.524 MHz
10b: 0.693 MHz 11b: 1.012 MHz

11. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable, DC (Double-byte command)	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1**
	1	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC

DC: Display ON/OFF (Default **0b: OFF**)

12. System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset (Double-byte command)	0	0	1	1	1	0	0	0	0	1
	1	0	1	1	1	0	0	0	1	0

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

13. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for “no operation”.

14. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double byte command)	0	0	1	1	1	0	0	1	0	TT
	1	0	For test only							

This command is used for UltraChip production testing. Please do *NOT* use.

15. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias Ratio. The ratio of V_{LCD} to V_{BIAS}.

00b:3 01b: 4 **10b: 5** 11b: 6

16. Set COM End (For Duty use)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [5:0] (Double-byte command)	0	0	1	1	1	1	0	0	0	1
	1	0	0	0	*CEN* register parameter					

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 64 pixel rows, the LCM designer should set CEN to *N-1* (where *N* is the number of pixel rows) and use COM1 through COM-*N* as COM driver electrodes. (Default: **63**)

17. Set LW

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LW (triple-byte command)	0	0	1	0	0	0	0	0	1	0
	1	0	0	0	0	0	0	0	0	0
	1	0	0	LW6	LW5	LW4	LW3	LW2	LW1	LW0

Number of SCLK per line

LW > 20; LW>(ISOF+ISOE+10) (**Default: 16H**)

18. Set ISOF

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set ISOF (triple-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	0	0	0	0	0	ISOF2	ISOF1	ISOF0

Number of COM Isolation clock in the front of the line.
ISOF+ISOE > 0 (**Default: 1H**)

19. Set ISOE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set ISOE (triple-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	1	0	0	0	0	0	0	ISOE2	ISOE1	ISOE0

Number of COM Isolation clock in the end of the line
ISOF+ISOE > 0 (**Default: 0H**)

20. Set CKC

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Clock Control, CKC (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
	1	0	0	0	0	CKC4	CKC3	CKC2	CKC1	CKC0

Clock Control:

CKC[4:0] : SCLK divider (**Default: 06H**)
000 0000b: SCLK frequency = MCLK
000 0001b~111 1111b: SCLK frequency = MCLK / CKC[4:0] / 2

LCD VOLTAGE SETTING

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_D, i.e.

$$BR = V_{LCD}/V_D,$$

where $V_D = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

UC1701e supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	3	4	**5**	6

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	**–0.00**	–0.05	–0.10	–0.15

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *TC* (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\,\%)$$

where

C_{V0} and C_{PM} are two constants,

PM is the numerical value of PM register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

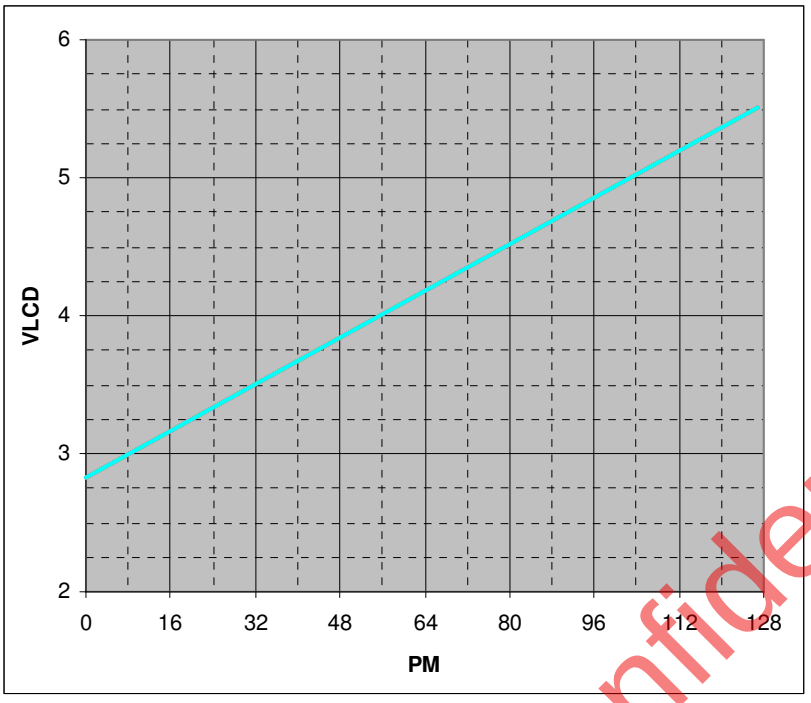
Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment or MTP is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1701e is designed to handle LCD panels with loading up to ~24nF using 20-Ω/Sq ITO glass with $V_{DD2/3} \geq 2.2V$. For larger LCD panels, use lower resistance ITO glass packaging.

V_{LCD} QUICK REFERENCE



V_{LCD} Programming Curve.

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} (V)	V_D(V)
3	2.825	21.12	0	2.83	0.94
			127	5.51	1.84
4	2.825	21.12	0	2.83	0.71
			127	5.51	1.38
5	2.825	21.12	0	2.83	0.57
			127	5.51	1.10
6	2.825	21.12	0	2.83	0.47
			127	5.51	0.92

Note:

1. For good product reliability, keep V_{LCD} under **5.51V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

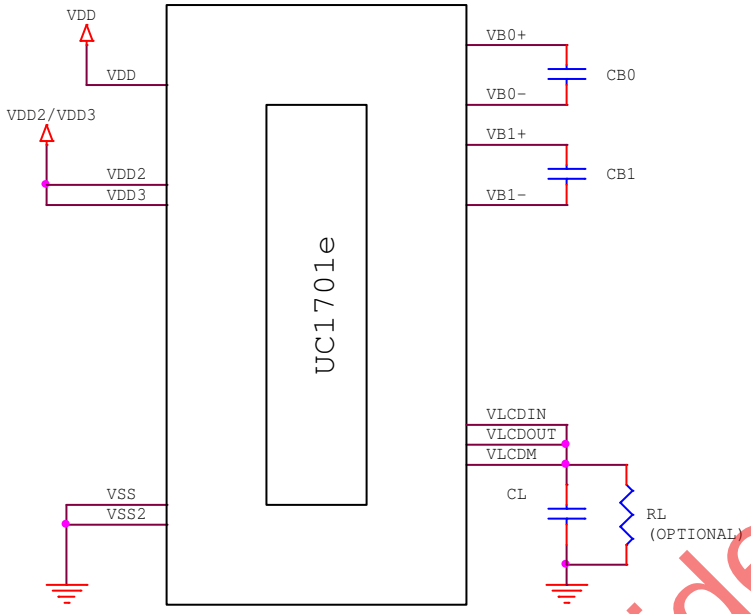


FIGURE 1.a: Reference circuit using Internal Hi-V generator circuit

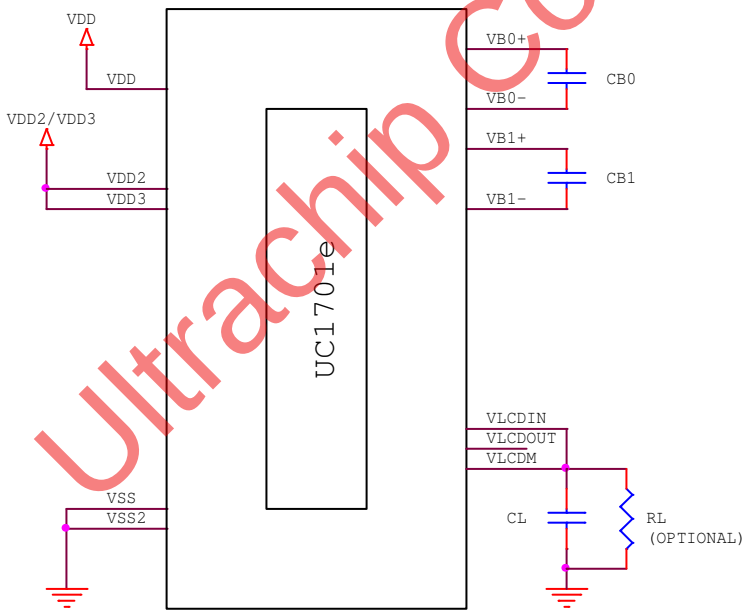


FIGURE 1.b: Reference circuit using External Hi-V generator circuit

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_{Bx} : 2.2 µF/5V or 300x LCD load capacitance, whichever is higher.

C_L : 330nF(16V) is appropriate for most applications.

R_L: 3.3M~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

All required components for the clock oscillator are built-in. No external parts are required.

SCLK: SCLK=MCLK/CKC[4:0]/2

Line Rate: LR = SCLK/LW

Frame Rate = LR/DUTY

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC). When SEG and COM drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM*x*, where x = 1~64, refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by CEN, MX or MY settings.

DISPLAY CONTROLS

There is a group of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC via *Set Display Enable* command. When DC is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1701e will put itself into Sleep Mode to conserve power.

When DC is set to ON, the DE flag will become "1", and UC1701e will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

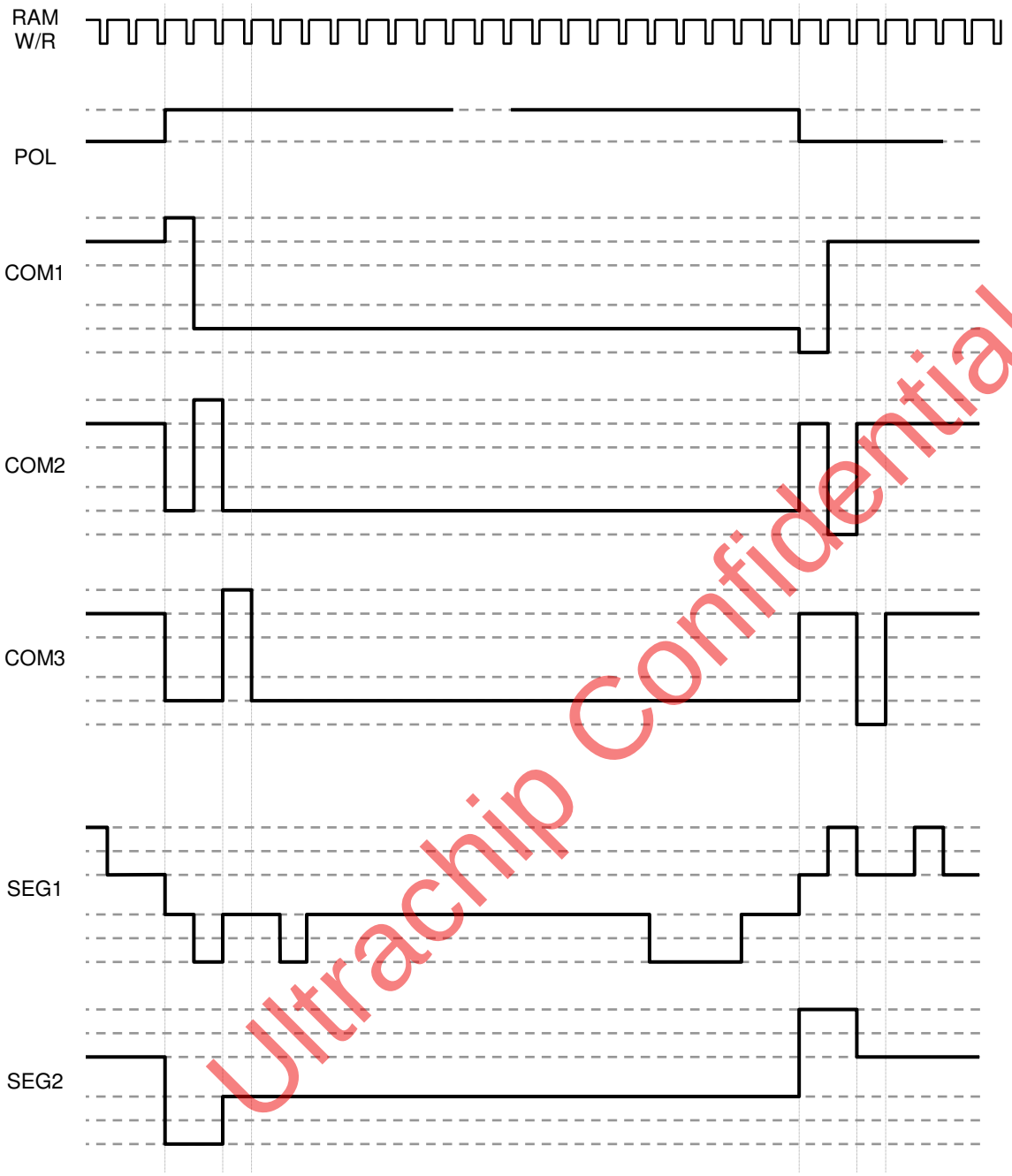


FIGURE 2: COM and SEG Electrode Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1701e supports 2 serial bus protocols. Designers can choose either a serial bus to create compact LCD modules and minimize connector pins.

		Serial Bus Type	
		S8(4-wire)	**S9(3-wire)**
Access		Read (status) / Write	
Control & Data Pins	BM	0	1
	CSB	Chip Select	
	CD	Control/Data	-
	SDA,SCK	SDA, SCK	

	CSB Disable Bus Interface	CSB Init. Bus State	RESET Init. Bus State
S8 or S9	✓	✓	✓

- CSB disable bus interface – CSB can be used to disable Bus Interface Write / Read Access.
- RESET can be pin reset / soft reset / power on reset.

Table 3: Host interfaces Summary

SERIAL INTERFACE

UC1701e supports two serial modes, a 4-wire SPI mode (S8) and a 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Pins CSB are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, these 8 bits will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

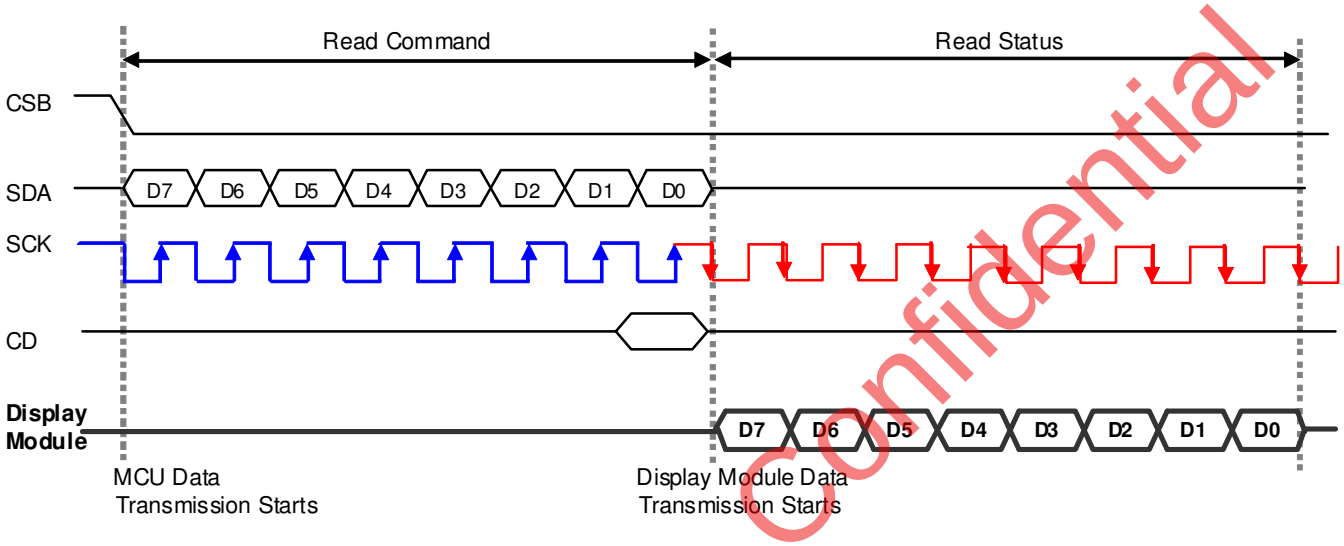


FIGURE 3.a: 4-wire Serial Interface (S8) – Read

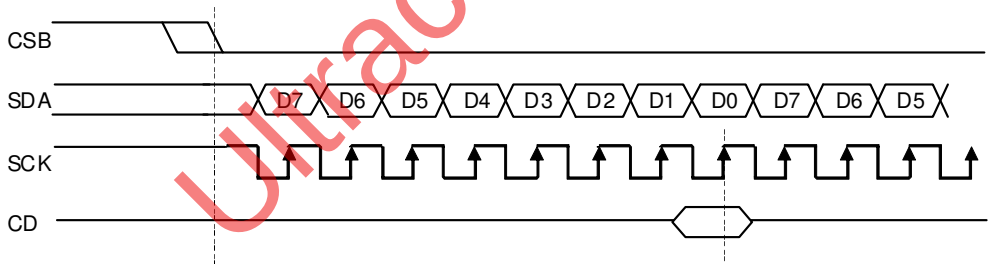


Figure 3.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIER) INTERFACE

Pins CSB are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CSB for each byte of data/command is recommended but optional.

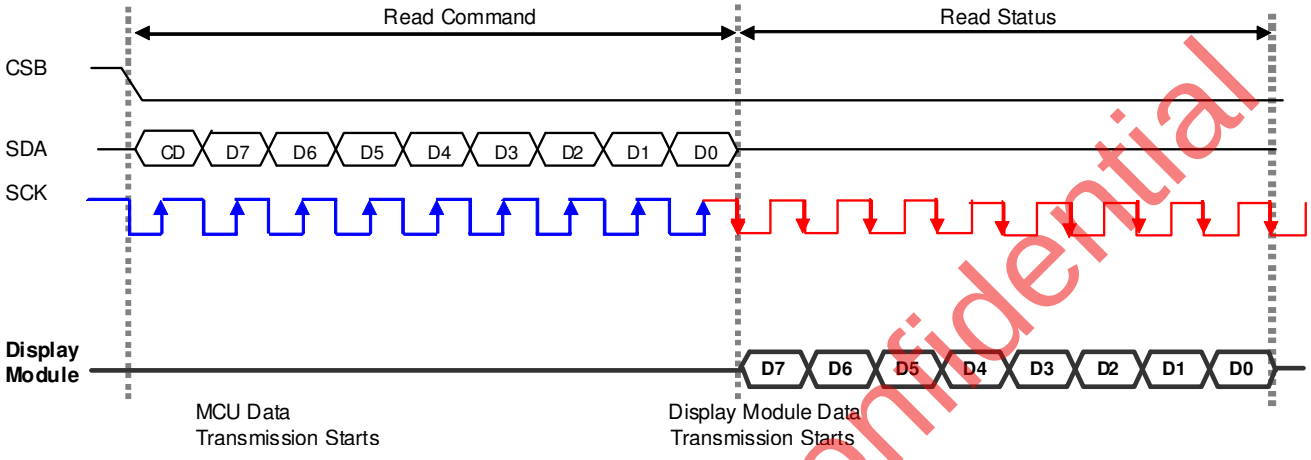


FIGURE 4.a: 3-wire Serial Interface (S9) – Read

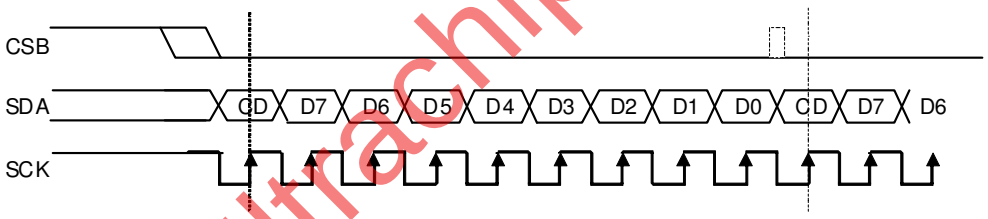


Figure 4.b: 3-wire Serial Interface (S9) – Write

HOST INTERFACE REFERENCE CIRCUIT

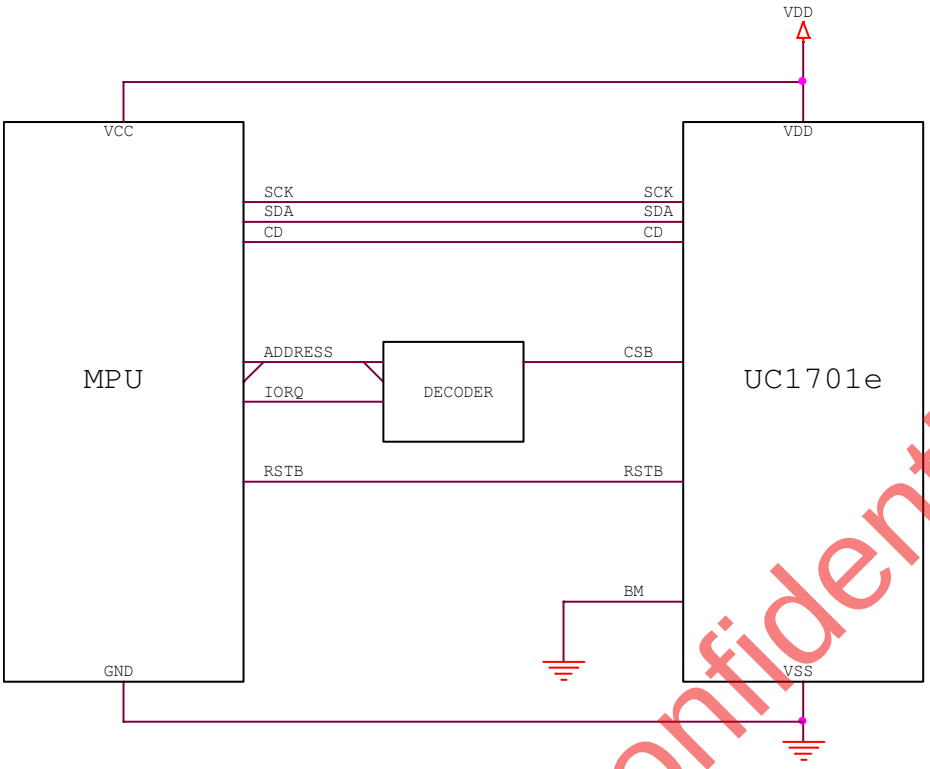


FIGURE 5: Serial-8 serial mode reference circuit

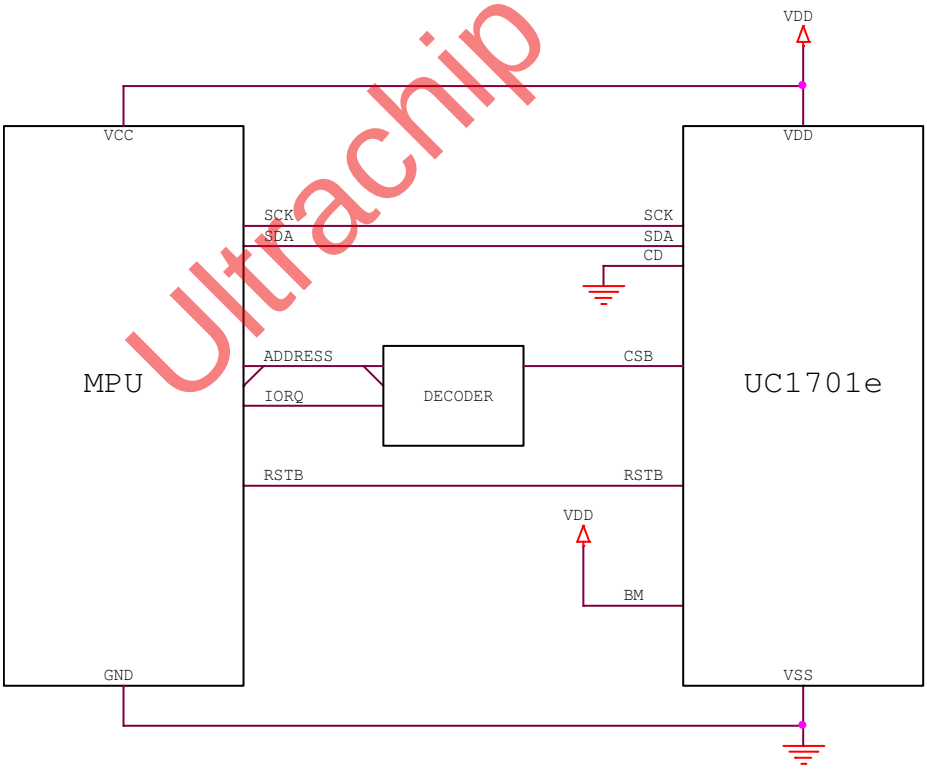


FIGURE 6: Serial-9 serial mode reference circuit

Note

- RSTB pin is optional. When the RSTB pin is not used, connect it to V_{DD}.
- R1, R2: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.

DISPLAY DATA RAM (DDRAM)

DATA ORGANIZATION

The input display data is stored to a dual port static DDRAM (DDRAM, for Display Data RAM) organized as 64x128.

After setting CA and RA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (127–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

$$Line = \text{Mod}(Line+1, 64)$$

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

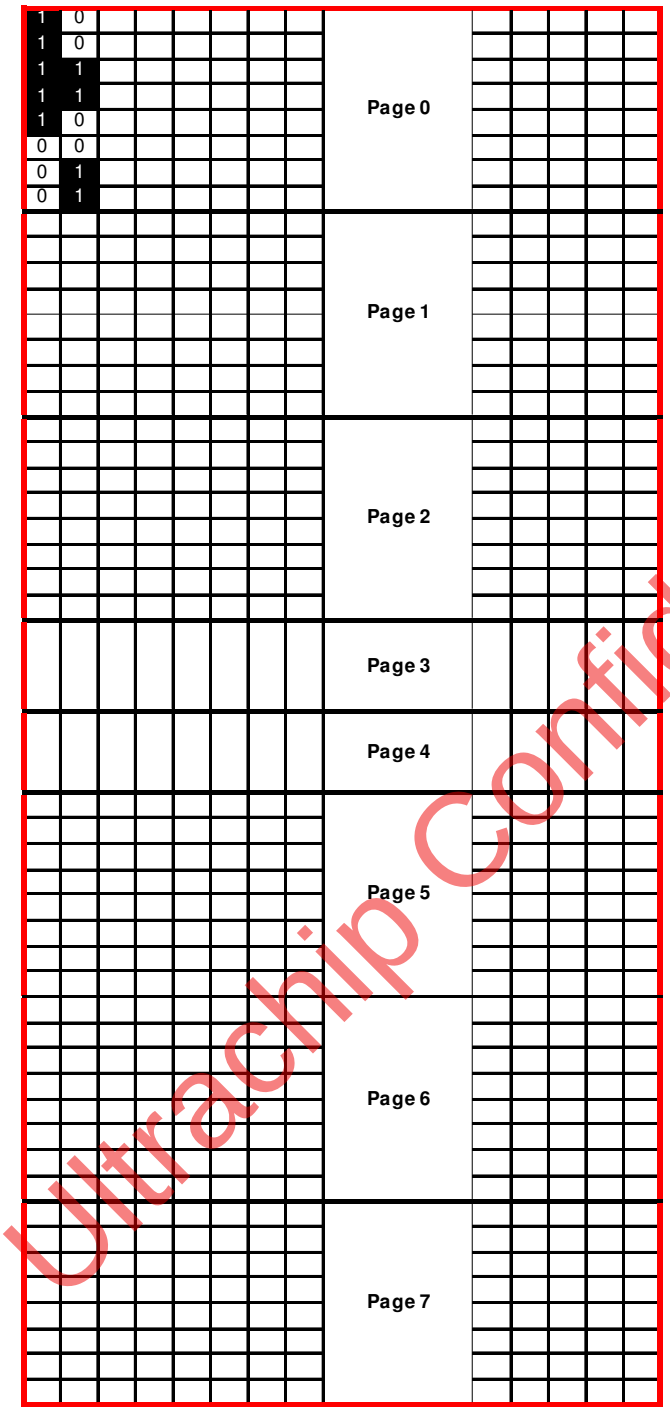
The above *Line* generation formula produce the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM.

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

PA[2:0]	0	Line Address
000	D0	R0
	D1	R1
	D2	R2
	D3	R3
	D4	R4
	D5	R5
	D6	R6
	D7	R7
001	D0	R8
	D1	R9
	D2	R10
	D3	R11
	D4	R12
	D5	R13
	D6	R14
	D7	R15
010	D0	R16
	D1	R17
	D2	R18
	D3	R19
	D4	R20
	D5	R21
	D6	R22
	D7	R23
011	:	:
100	:	:
101	D0	R40
	D1	R41
	D2	R42
	D3	R43
	D4	R44
	D5	R45
	D6	R46
	D7	R47
110	D0	R48
	D1	R49
	D2	R50
	D3	R51
	D4	R52
	D5	R53
	D6	R54
	D7	R55
111	D0	R56
	D1	R57
	D2	R58
	D3	R59
	D4	R60
	D5	R61
	D6	R62
	D7	R63



Panel Location	MY=0	MY=1
COM1	R0	R63
COM2	R1	R62
COM3	R2	R61
COM4	R3	R60
COM5	R4	R59
COM6	R5	R58
COM7	R6	R57
COM8	R7	R56
COM9	R8	R55
COM10	R9	R54
COM11	R10	R53
COM12	R11	R52
COM13	R12	R51
COM14	R13	R50
COM15	R14	R49
COM16	R15	R48
COM17	R16	R47
COM18	R17	R46
COM19	R18	R45
COM20	R19	R44
COM21	R20	R43
COM22	R21	R42
COM23	R22	R41
COM24	R23	R40
:	:	:
:	:	:
COM41	R40	R23
COM42	R41	R22
COM43	R42	R21
COM44	R43	R20
COM45	R44	R19
COM46	R45	R18
COM47	R46	R17
COM48	R47	R16
COM49	R48	R15
COM50	R49	R14
COM51	R50	R13
COM52	R51	R12
COM53	R52	R11
COM54	R53	R10
COM55	R54	R9
COM56	R55	R8
COM57	R56	R7
COM58	R57	R6
COM59	R58	R5
COM60	R59	R4
COM61	R60	R3
COM62	R61	R2
COM63	R62	R1
COM64	R63	R0

MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG124	SEG125	SEG126	SEG127	SEG128
MX=1	SEG128	SEG127	SEG126	SEG125	SEG124	SEG123	SEG122	SEG121		SEG5	SEG4	SEG3	SEG2	SEG1

Example for memory mapping: let MX = 0, MY = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 (D7-D0) : 0001 1111b
⇒ Page 0 SEG 2 (D7-D0) : 1100 1100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1701e has two different types of Reset: *Pin Reset* (hardware reset) and *System-Reset* (software reset). *Pin Reset* is activated by connecting the RST pin to ground; while *System Reset* is performed by software commands.

After each power-up, a *Pin Reset* is required after waiting for 3mS.

In the following discussions, reset means *Pin Reset*.

The differences between pin reset and software reset are

Procedure (Restoring to default value)	Pin Reset (Hardware)	System Reset (Software)
Column Address : CA[6:0]=0	V	V
Page Address : PA[2:0]=0	V	V
Temp. Compensation : TC[1:0]=00b	V	X
Power Control : PC[2:0]=101b	V	X
VBIAS Potentiometer : PM[6:0]=6Eh	V	X
Display Enable : DC=0b	V	X
LCD Mapping Control : LC[3:0]=0010b	V	X
LCD Bias Ratio : BR[1:0]=10b	V	X
COM End : CEN[5:0]=63d	V	X

RESET STATUS

When UC1701e enters RESET sequence:

- Operation mode will be “Reset”
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1701e has three operating modes (OM): Reset, Sleep, Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1701e's internal clock. To ensure consistent system states, wait at least 10µS after issuing the `Set Display Enable` command or triggering `System Reset`.

Action	Mode	OM
RSTB pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1701e consumes very little energy in Sleep mode (typically under 5µA).

EXITING SLEEP MODE

UC1701e contains internal logic to check whether V_{LCD} and V_D are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1701e internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

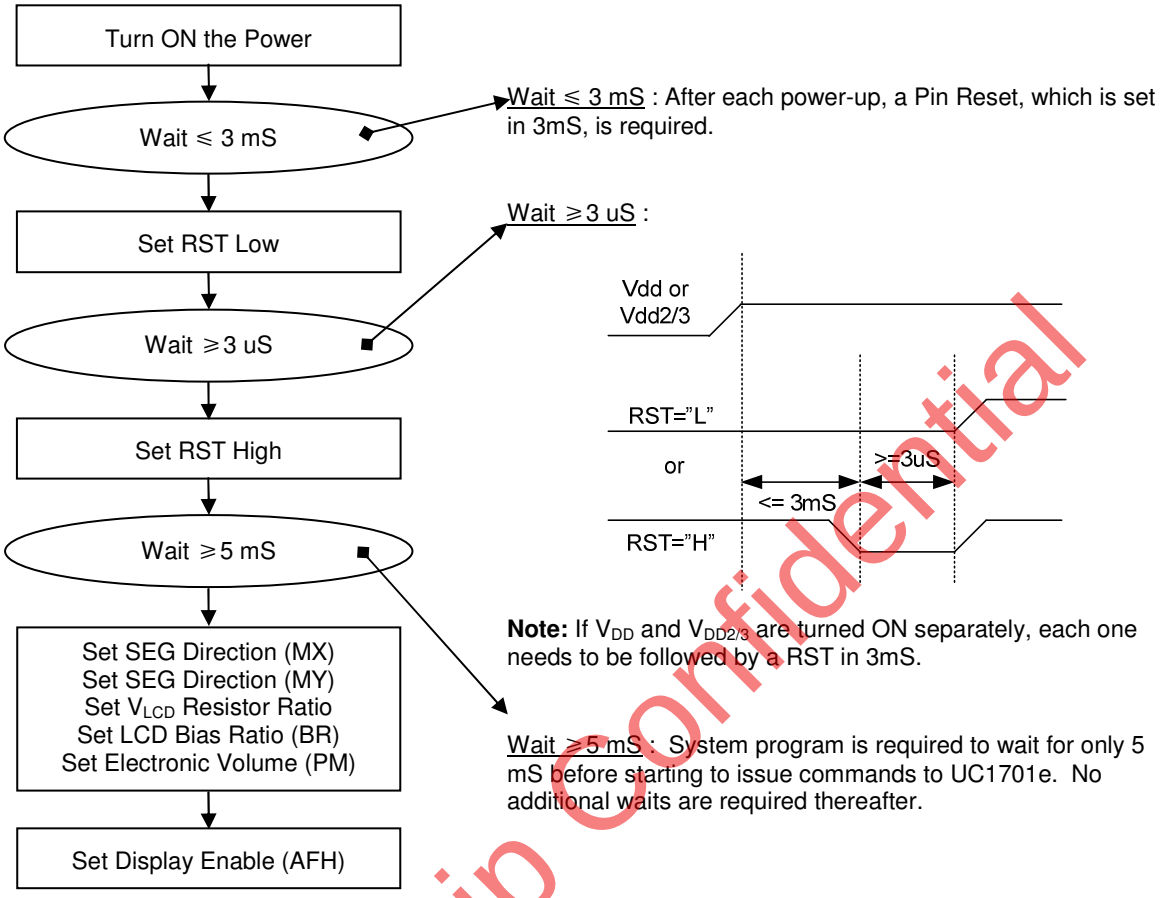


Figure 7: Reference Power-Up Sequence

There's no delay needed while turning ON V_{DD} and $V_{DD2/3}$, and either one can be turned ON first.

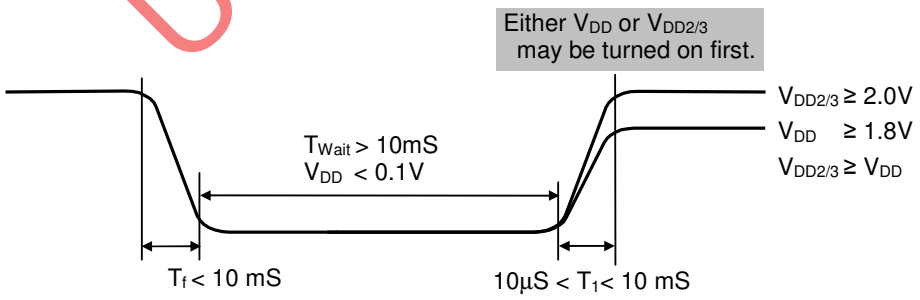


Figure 8: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1701e enters Sleep mode from Display mode by issuing Set Display Disable command and setting all-pixel-ON.

To exit Sleep mode, set All-pixel-OFF.

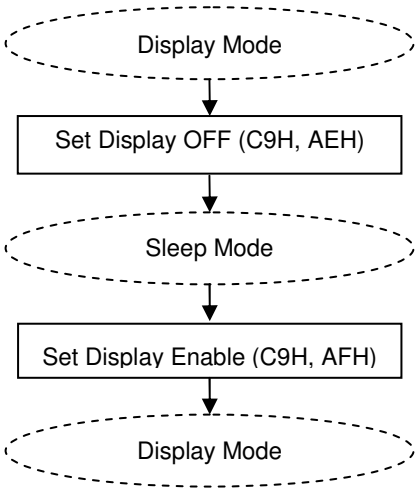


FIGURE 9: Reference Enter/Exit Sleep Mode Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

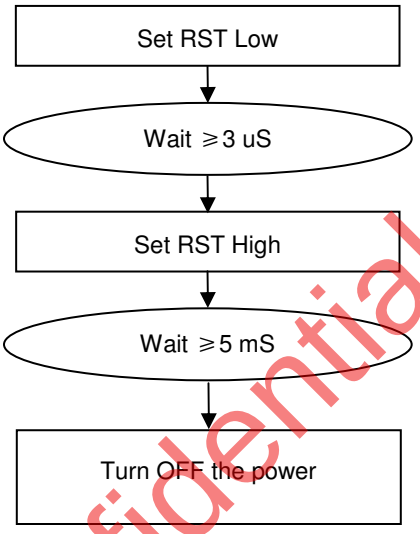


FIGURE 10: Reference Power-Down Sequence

SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R											Wait ≤ 3 mS	
R											Set RSTB pin Low	Wait 3 uS after RST is Low
R											Set RSTB pin High	Wait 150mS after RST is High
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, Master Clock.
R	0	0	0	0	1	0	1	#	#	#	Set Power Control	
R	0	0	1	0	1	0	#	#	#	#	Set LCD	
R	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	
R	0 1	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	LCD specific operating voltage setting
O	0 1 . . 1	0 0 . . 0	0 # . . #	0 # . . #	0 # . . #	0 # . . #	0 # . . #	0 # . . #	0 # . . #	1 # . . #	Write display RAM	Set up display image
R	0 1	0 0	1 1	1 0	0 1	0 0	1 1	0 1	0 1	1 1	Set Display Enable	

* Issue the commands in blue color only when using MTP functions.

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R											Set RSTB pin Low	Wait 3 uS after RST is Low
R											Set RSTB pin High	
R											Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0 1	0 0	1 1	1 0	0 1	0 0	1 1	0 1	0 1	1 0	Set Display Disable	
O	0 1 . . 1	0 0 . . 0	0 # . . #	0 # . . #	0 # . . #	0 # . . #	0 # . . #	0 # . . #	0 # . . #	1 # . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0 0	0 0	1 1	1 0	0 1	0 0	1 1	0 0	0 1	1 1	Set Display Enable	

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 – notes 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.2	V
V_{LCD}	LCD Generated voltage	-0.3	+5.7	V
V_{IN} / V_{OUT}	Any input/output	-0.4	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-40	+85	°C
T_{STR}	Storage temperature	-55	+125	°C

Notes

1. V_{DD} is based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.8	2.0~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.0	2.2~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant$ 2.0V, 25°C	2.83	5.11	5.51	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant$ 2.0V, 25°C	0.8	-	1.208	V
V_{IL}	Input logic LOW	V_{DD} =1.8V ~ 2.5V			$0.1V_{DD}$	V
		V_{DD} =2.5V ~ 3.6V			$0.2V_{DD}$	
V_{IH}	Input logic HIGH	V_{DD} =1.8V ~ 2.5V	$0.9V_{DD}$			V
		V_{DD} =2.5V ~ 3.6V	$0.8V_{DD}$			
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	µA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3}$ = 3.3V, Temp = 85°C		10		µA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 5V		1.10	1.80	Ω
$R_{0(COM)}$	COM output impedance	V_{LCD} = 5V		1.10	1.80	Ω
F_{FR}	Average Frame Rate		-10%	40.7	+10%	Hz

POWER CONSUMPTION

V_{DD} = 3V,
V_{LCD} = 5.11V
Mux Rate = 64,
Temperature = 25°C,
Bias Ratio = 10b,
Frame Rate = 10Hz
Bus mode =S8,
C_L = 330nF,
PM = 6EH,
C_B = 2.2µF,
All outputs are open circuit.

Display Pattern	Conditions	Typ.	Max.
All-ON	Bus = idle	32	48
All-OFF	Bus = idle	31	46.5
2-pixel checker	Bus = idle	34	51
-	Bus = idle (standby current)	-	5

AC CHARACTERISTICS

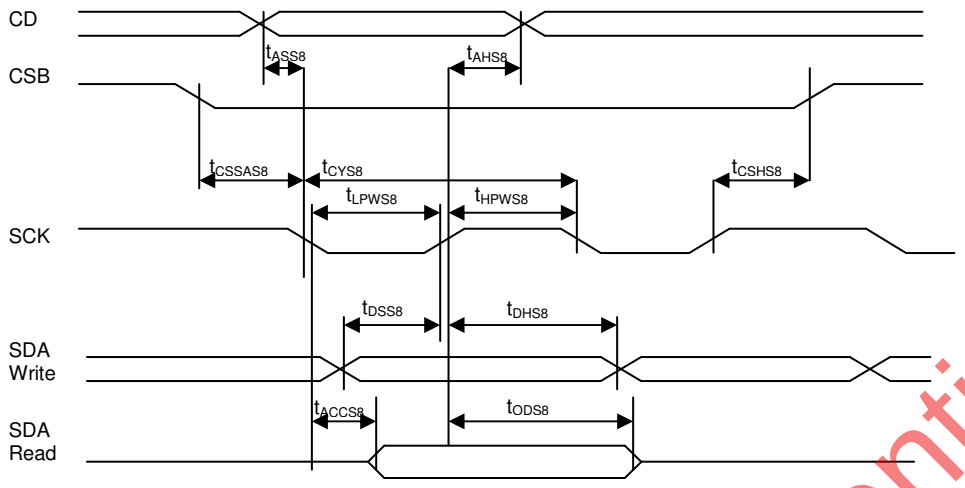


FIGURE 11: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} ≤ 3.6V, Ta= –40 to +85°C)				(Read / Write)		
t_{ASS8}	CD	Address setup time		5	–	nS
t_{AHS8}		Address hold time		10		
t_{CSSAS8}	CSB	Chip select setup time		5	–	nS
t_{CSHS8}		Chip select hold time		50		
t_{CYS8}	SCK	System Cycle time		190 / 130	–	nS
t_{LPWS8}		Low pulse width		80 / 50		
t_{HPWS8}		High pulse width		80 / 50		
t_{DSS8}	SDA (Write)	Data setup time		30	–	nS
t_{DHS8}		Data hold time		10		
t_{ACC8}	SDA (Read)	Read access time	C_L = 100pF	–	80	nS
t_{OD8}		Output disable time		30	–	
(1.8V ≤ V_{DD} < 2.5V, Ta= –40 to +85°C)				(Read / Write)		
t_{ASS8}	CD	Address setup time		5	–	nS
t_{AHS8}		Address hold time		10		
t_{CSSAS8}	CSB	Chip select setup time		15	–	nS
t_{CSHS8}		Chip select hold time		90		
t_{CYS8}	SCK	System Cycle time		230 / 120	–	nS
t_{LPWS8}		Low pulse width		100 / 90	–	nS
t_{HPWS8}		High pulse width		100 / 90	–	nS
t_{DSS8}	SDA (Write)	Data setup time		30	–	nS
t_{DHS8}		Data hold time		10		
t_{ACC8}	SDA (Read)	Read access time	C_L = 100pF	–	100	nS
t_{OD8}		Output disable time		60	–	

Note: tr (Rising time), tf (falling time) : ≤ 15nS

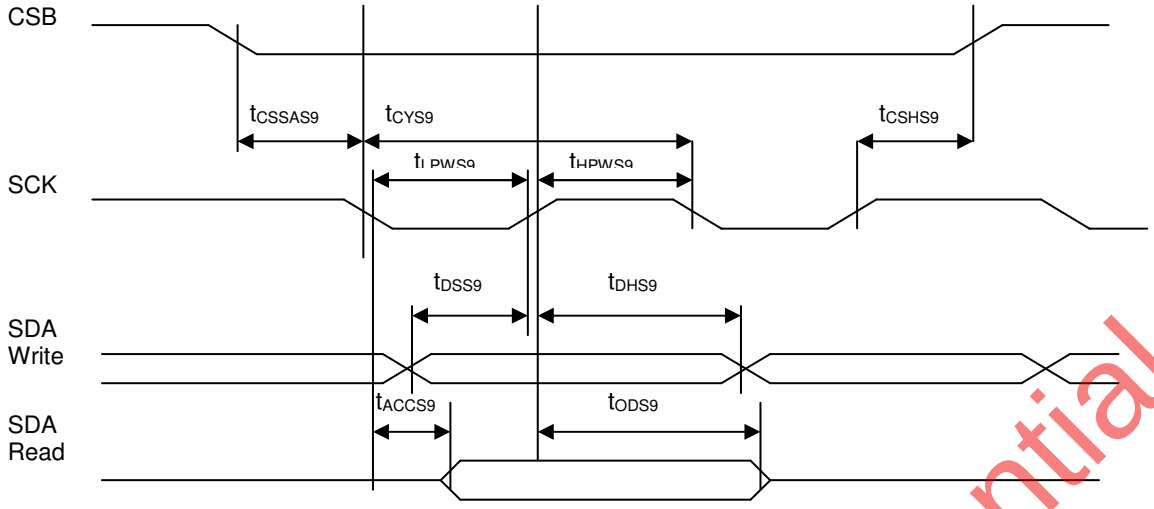


FIGURE 12: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ⩽ V_{DD} ⩽ 3.6V, Ta= –40 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CSB	Chip select setup time Chip select hold time		5 50	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		190 / 130 80 / 50 80 / 50	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		30 10	–	nS
t_{ACC9} t_{OD9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– 30	80 –	nS
(1.8V ⩽ V_{DD} < 2.5V, Ta= –40 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CSB	Chip select setup time		10 90	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		230 / 120 100 / 90 100 / 90	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		30 10	–	nS
t_{ACC9} t_{OD9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– 60	100 –	nS

Note: tr (Rising time), tf (falling time) : ⩽ 15nS

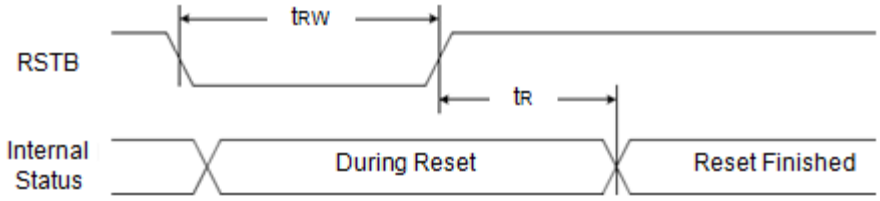


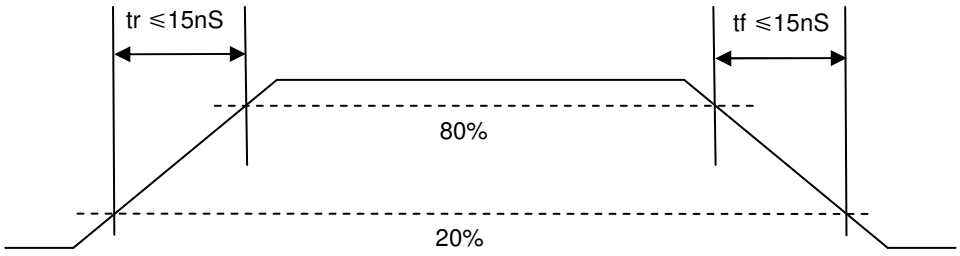
FIGURE 13: Reset Characteristics

(1.8V ⩽ V_{DD} ⩽ 3.6V, Ta= –40 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
t_{RW}	RSTB	Reset low pulse width		3	–	µS
t_R	RST, Internal Status	Reset to Internal Status pulse delay		6	–	mS

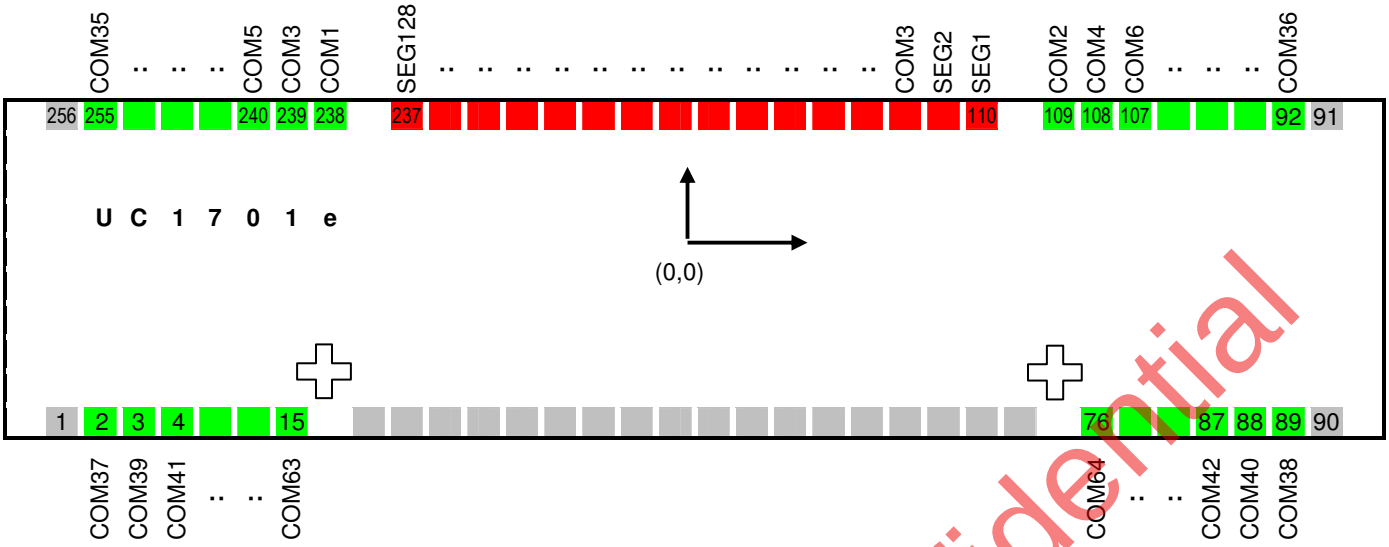
Note:

For each mode, the signal's rising and falling times (tr, tf) are stipulated to be equal to or less than 15nS each.



PHYSICAL DIMENSIONS

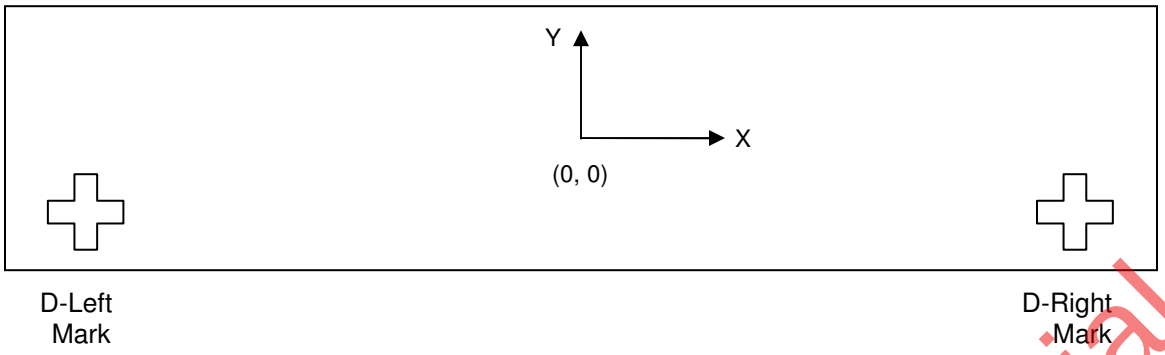
Circuit / Bump View:



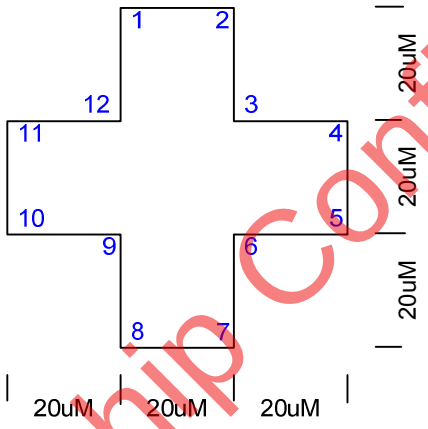
Die Size:	4190 µM x 570 µM ± 30 µM
Die Thickness:	300 µM ± 20 µM
Die TTV:	$(D_{MAX} – D_{MIN})$ within die ≤ 2 µM
Bump Height:	9 µM ± 3 µM (Part Number: UC1701eGAA)
	15 µM ± 3 µM (Part Number: UC1701eGBA)
	$(H_{MAX} – H_{MIN})$ within die ≤ 3 µM
Bump Size:	12 µM x 125 µM ± 3 µM
Bump Pitch:	24 µM
Bump Gap:	12 µM ± 4 µM
Bump Area:	1500 $µM^2$
Coordinate origin:	Chip center
Pad reference:	Pad center

ALIGNMENT MARK INFORMATION

Mark Locations:



Shape and Points:



Coordinates:

Point	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1	-1655	-188	1624	-188
2	-1635	-188	1644	-188
3	-1635	-208	1644	-208
4	-1615	-208	1664	-208
5	-1615	-228	1664	-228
6	-1635	-228	1644	-228
7	-1635	-248	1644	-248
8	-1655	-248	1624	-248
9	-1655	-228	1624	-228
10	-1675	-228	1604	-228
11	-1675	-208	1604	-208
12	-1655	-208	1624	-208

PAD COORDINATES

No.	Pad_Name	X	Y	W	H
1	DUMMY2	-2056.5	-202.5	15	125
2	COM_PAD<37>	-2029.5	-202.5	15	125
3	COM_PAD<39>	-2002.5	-202.5	15	125
4	COM_PAD<41>	-1977	-202.5	12	125
5	COM_PAD<43>	-1953	-202.5	12	125
6	COM_PAD<45>	-1929	-202.5	12	125
7	COM_PAD<47>	-1905	-202.5	12	125
8	COM_PAD<49>	-1881	-202.5	12	125
9	COM_PAD<51>	-1857	-202.5	12	125
10	COM_PAD<53>	-1833	-202.5	12	125
11	COM_PAD<55>	-1809	-202.5	12	125
12	COM_PAD<57>	-1785	-202.5	12	125
13	COM_PAD<59>	-1761	-202.5	12	125
14	COM_PAD<61>	-1737	-202.5	12	125
15	COM_PAD<63>	-1713	-202.5	12	125
16	DUMMY	-1551.8	-223.3	50.2	81.4
17	CSB_PAD	-1484.9	-223.3	45.8	81.4
18	VSSX	-1421.9	-223.3	45.8	81.4
19	BM_PAD	-1358.9	-223.3	45.8	81.4
20	RSTB_PAD	-1293.7	-223.3	45.8	81.4
21	DUMMY	-1225	-223.3	45.8	81.4
22	CD_PAD	-1156.3	-223.3	45.8	81.4
23	SCK_PAD	-1091.1	-223.3	45.8	81.4
24	DUMMY	-1022.6	-223.3	45.8	81.4
25	SDA_PAD	-954.1	-223.3	45.8	81.4
26	DUMMY	-894.2	-223.3	44	81.4
27	TST2_PAD	-833.65	-223.3	45.8	81.4
28	VDD3	-771.1	-225	33	78
29	VDD3	-723.1	-225	33	78
30	VDD3	-675.1	-225	33	78
31	VDD3	-627.1	-225	33	78
32	VDD2	-579.1	-225	33	78
33	VDD2	-531.1	-225	33	78
34	VDD2	-483.1	-225	33	78
35	VDD2	-435.1	-225	33	78
36	VDD	-387.1	-225	33	78
37	VDD	-339.1	-225	33	78
38	VDD	-291.1	-225	33	78
39	VDD	-243.1	-225	33	78
40	VDD	-195.1	-225	33	78
41	VSS2	-147.1	-225	33	78
42	VSS2	-99.1	-225	33	78
43	VSS2	-51.1	-225	33	78
44	VSS2	-3.1	-225	33	78

No.	Pad_Name	X	Y	W	H
45	VSS	44.9	-225	33	78
46	VSS	92.9	-225	33	78
47	VSS	140.9	-225	33	78
48	VSS	188.9	-225	33	78
49	VSS	236.9	-225	33	78
50	VBN_PAD<0>	284.9	-225	33	78
51	VBN_PAD<0>	332.9	-225	33	78
52	VBN_PAD<0>	380.9	-225	33	78
53	VBN_PAD<1>	428.9	-225	33	78
54	VBN_PAD<1>	476.9	-225	33	78
55	VBN_PAD<1>	524.9	-225	33	78
56	VBP_PAD<1>	573.5	-225	33	78
57	VBP_PAD<1>	621.5	-225	33	78
58	VBP_PAD<1>	669.5	-225	33	78
59	VBP_PAD<0>	717.5	-225	33	78
60	VBP_PAD<0>	765.5	-225	33	78
61	VBP_PAD<0>	813.5	-225	33	78
62	VLCDIN_PAD	862.1	-225	33	78
63	VLCDIN_PAD	910.1	-225	33	78
64	VLCDIN_PAD	958.1	-225	33	78
65	VLCDM_PAD	1058.55	-225	33	78
66	VLCDM_PAD	1106.55	-225	33	78
67	VLCDM_PAD	1154.55	-225	33	78
68	VLCDOUT_PAD	1203.15	-225	33	78
69	VLCDOUT_PAD	1251.15	-225	33	78
70	VLCDOUT_PAD	1299.15	-225	33	78
71	VLCDOUT_PAD	1347.15	-225	33	78
72	VLCDOUT_PAD	1395.15	-225	33	78
73	DUMMY	1443.15	-225	33	78
74	DUMMY	1491.15	-225	33	78
75	DUMMY	1539.15	-225	33	78
76	COM_PAD<64>	1713	-202.5	12	125
77	COM_PAD<62>	1737	-202.5	12	125
78	COM_PAD<60>	1761	-202.5	12	125
79	COM_PAD<58>	1785	-202.5	12	125
80	COM_PAD<56>	1809	-202.5	12	125
81	COM_PAD<54>	1833	-202.5	12	125
82	COM_PAD<52>	1857	-202.5	12	125
83	COM_PAD<50>	1881	-202.5	12	125
84	COM_PAD<48>	1905	-202.5	12	125
85	COM_PAD<46>	1929	-202.5	12	125
86	COM_PAD<44>	1953	-202.5	12	125
87	COM_PAD<42>	1977	-202.5	12	125
88	COM_PAD<40>	2002.5	-202.5	15	125

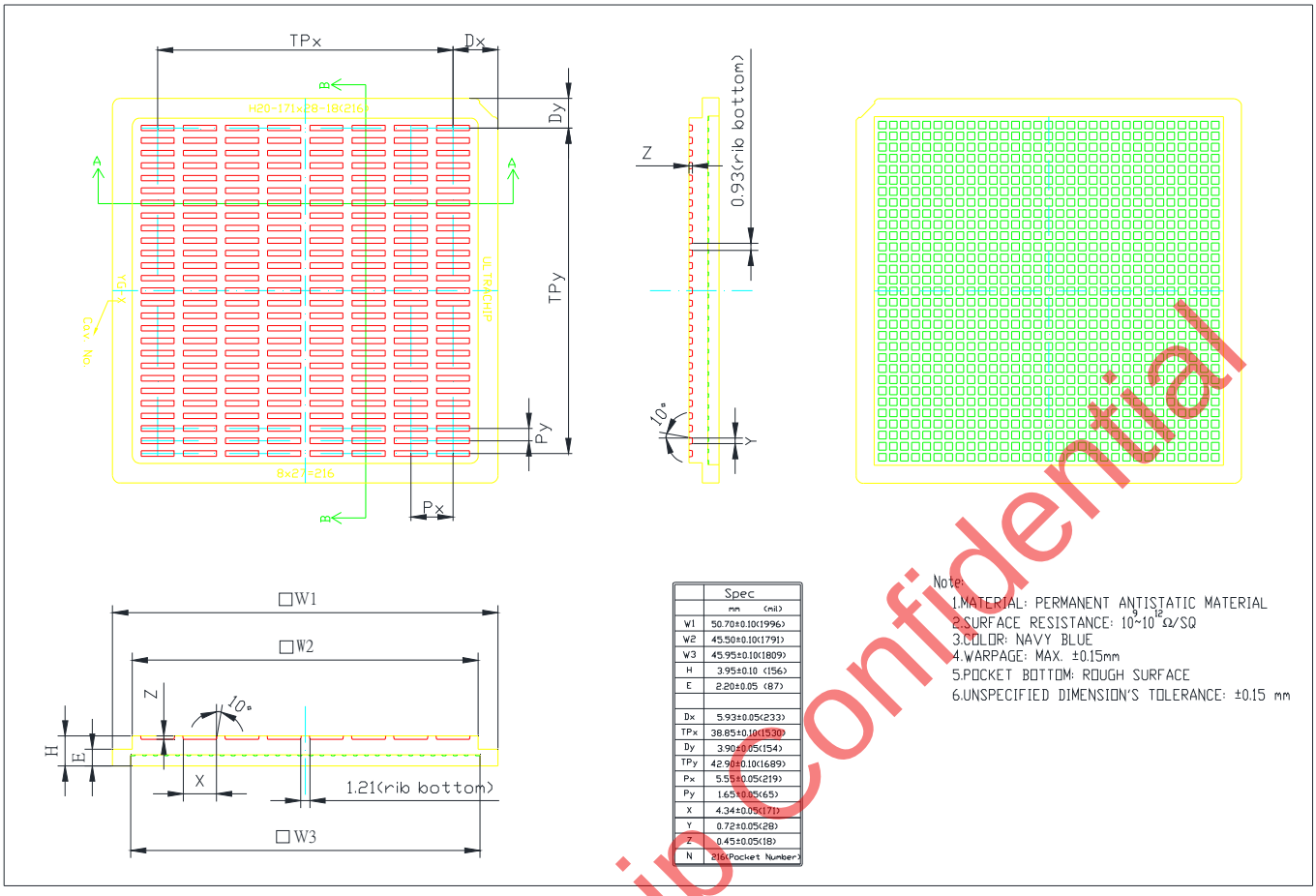
No.	Pad_Name	X	Y	W	H
89	COM_PAD<38>	2029.5	-202.5	15	125
90	DUMMY3	2056.5	-202.5	15	125
91	DUMMY4	2058	202.5	12	125
92	COM_PAD<36>	2034	202.5	12	125
93	COM_PAD<34>	2010	202.5	12	125
94	COM_PAD<32>	1986	202.5	12	125
95	COM_PAD<30>	1962	202.5	12	125
96	COM_PAD<28>	1938	202.5	12	125
97	COM_PAD<26>	1914	202.5	12	125
98	COM_PAD<24>	1890	202.5	12	125
99	COM_PAD<22>	1866	202.5	12	125
100	COM_PAD<20>	1842	202.5	12	125
101	COM_PAD<18>	1818	202.5	12	125
102	COM_PAD<16>	1794	202.5	12	125
103	COM_PAD<14>	1770	202.5	12	125
104	COM_PAD<12>	1746	202.5	12	125
105	COM_PAD<10>	1722	202.5	12	125
106	COM_PAD<8>	1698	202.5	12	125
107	COM_PAD<6>	1674	202.5	12	125
108	COM_PAD<4>	1650	202.5	12	125
109	COM_PAD<2>	1626	202.5	12	125
110	SEG_PAD<1>	1526	202.5	12	125
111	SEG_PAD<2>	1502	202.5	12	125
112	SEG_PAD<3>	1478	202.5	12	125
113	SEG_PAD<4>	1454	202.5	12	125
114	SEG_PAD<5>	1430	202.5	12	125
115	SEG_PAD<6>	1406	202.5	12	125
116	SEG_PAD<7>	1382	202.5	12	125
117	SEG_PAD<8>	1358	202.5	12	125
118	SEG_PAD<9>	1334	202.5	12	125
119	SEG_PAD<10>	1310	202.5	12	125
120	SEG_PAD<11>	1286	202.5	12	125
121	SEG_PAD<12>	1262	202.5	12	125
122	SEG_PAD<13>	1238	202.5	12	125
123	SEG_PAD<14>	1214	202.5	12	125
124	SEG_PAD<15>	1190	202.5	12	125
125	SEG_PAD<16>	1166	202.5	12	125
126	SEG_PAD<17>	1142	202.5	12	125
127	SEG_PAD<18>	1118	202.5	12	125
128	SEG_PAD<19>	1094	202.5	12	125
129	SEG_PAD<20>	1070	202.5	12	125
130	SEG_PAD<21>	1046	202.5	12	125
131	SEG_PAD<22>	1022	202.5	12	125
132	SEG_PAD<23>	998	202.5	12	125
133	SEG_PAD<24>	974	202.5	12	125

No.	Pad_Name	X	Y	W	H
134	SEG_PAD<25>	950	202.5	12	125
135	SEG_PAD<26>	926	202.5	12	125
136	SEG_PAD<27>	902	202.5	12	125
137	SEG_PAD<28>	878	202.5	12	125
138	SEG_PAD<29>	854	202.5	12	125
139	SEG_PAD<30>	830	202.5	12	125
140	SEG_PAD<31>	806	202.5	12	125
141	SEG_PAD<32>	782	202.5	12	125
142	SEG_PAD<33>	758	202.5	12	125
143	SEG_PAD<34>	734	202.5	12	125
144	SEG_PAD<35>	710	202.5	12	125
145	SEG_PAD<36>	686	202.5	12	125
146	SEG_PAD<37>	662	202.5	12	125
147	SEG_PAD<38>	638	202.5	12	125
148	SEG_PAD<39>	614	202.5	12	125
149	SEG_PAD<40>	590	202.5	12	125
150	SEG_PAD<41>	566	202.5	12	125
151	SEG_PAD<42>	542	202.5	12	125
152	SEG_PAD<43>	518	202.5	12	125
153	SEG_PAD<44>	494	202.5	12	125
154	SEG_PAD<45>	470	202.5	12	125
155	SEG_PAD<46>	446	202.5	12	125
156	SEG_PAD<47>	422	202.5	12	125
157	SEG_PAD<48>	398	202.5	12	125
158	SEG_PAD<49>	374	202.5	12	125
159	SEG_PAD<50>	350	202.5	12	125
160	SEG_PAD<51>	326	202.5	12	125
161	SEG_PAD<52>	302	202.5	12	125
162	SEG_PAD<53>	278	202.5	12	125
163	SEG_PAD<54>	254	202.5	12	125
164	SEG_PAD<55>	230	202.5	12	125
165	SEG_PAD<56>	206	202.5	12	125
166	SEG_PAD<57>	182	202.5	12	125
167	SEG_PAD<58>	158	202.5	12	125
168	SEG_PAD<59>	134	202.5	12	125
169	SEG_PAD<60>	110	202.5	12	125
170	SEG_PAD<61>	86	202.5	12	125
171	SEG_PAD<62>	62	202.5	12	125
172	SEG_PAD<63>	38	202.5	12	125
173	SEG_PAD<64>	14	202.5	12	125
174	SEG_PAD<65>	-10	202.5	12	125
175	SEG_PAD<66>	-34	202.5	12	125
176	SEG_PAD<67>	-58	202.5	12	125
177	SEG_PAD<68>	-82	202.5	12	125
178	SEG_PAD<69>	-106	202.5	12	125

No.	Pad_Name	X	Y	W	H
179	SEG_PAD<70>	-130	202.5	12	125
180	SEG_PAD<71>	-154	202.5	12	125
181	SEG_PAD<72>	-178	202.5	12	125
182	SEG_PAD<73>	-202	202.5	12	125
183	SEG_PAD<74>	-226	202.5	12	125
184	SEG_PAD<75>	-250	202.5	12	125
185	SEG_PAD<76>	-274	202.5	12	125
186	SEG_PAD<77>	-298	202.5	12	125
187	SEG_PAD<78>	-322	202.5	12	125
188	SEG_PAD<79>	-346	202.5	12	125
189	SEG_PAD<80>	-370	202.5	12	125
190	SEG_PAD<81>	-394	202.5	12	125
191	SEG_PAD<82>	-418	202.5	12	125
192	SEG_PAD<83>	-442	202.5	12	125
193	SEG_PAD<84>	-466	202.5	12	125
194	SEG_PAD<85>	-490	202.5	12	125
195	SEG_PAD<86>	-514	202.5	12	125
196	SEG_PAD<87>	-538	202.5	12	125
197	SEG_PAD<88>	-562	202.5	12	125
198	SEG_PAD<89>	-586	202.5	12	125
199	SEG_PAD<90>	-610	202.5	12	125
200	SEG_PAD<91>	-634	202.5	12	125
201	SEG_PAD<92>	-658	202.5	12	125
202	SEG_PAD<93>	-682	202.5	12	125
203	SEG_PAD<94>	-706	202.5	12	125
204	SEG_PAD<95>	-730	202.5	12	125
205	SEG_PAD<96>	-754	202.5	12	125
206	SEG_PAD<97>	-778	202.5	12	125
207	SEG_PAD<98>	-802	202.5	12	125
208	SEG_PAD<99>	-826	202.5	12	125
209	SEG_PAD<100>	-850	202.5	12	125
210	SEG_PAD<101>	-874	202.5	12	125
211	SEG_PAD<102>	-898	202.5	12	125
212	SEG_PAD<103>	-922	202.5	12	125
213	SEG_PAD<104>	-946	202.5	12	125
214	SEG_PAD<105>	-970	202.5	12	125
215	SEG_PAD<106>	-994	202.5	12	125
216	SEG_PAD<107>	-1018	202.5	12	125
217	SEG_PAD<108>	-1042	202.5	12	125
218	SEG_PAD<109>	-1066	202.5	12	125

No.	Pad_Name	X	Y	W	H
219	SEG_PAD<110>	-1090	202.5	12	125
220	SEG_PAD<111>	-1114	202.5	12	125
221	SEG_PAD<112>	-1138	202.5	12	125
222	SEG_PAD<113>	-1162	202.5	12	125
223	SEG_PAD<114>	-1186	202.5	12	125
224	SEG_PAD<115>	-1210	202.5	12	125
225	SEG_PAD<116>	-1234	202.5	12	125
226	SEG_PAD<117>	-1258	202.5	12	125
227	SEG_PAD<118>	-1282	202.5	12	125
228	SEG_PAD<119>	-1306	202.5	12	125
229	SEG_PAD<120>	-1330	202.5	12	125
230	SEG_PAD<121>	-1354	202.5	12	125
231	SEG_PAD<122>	-1378	202.5	12	125
232	SEG_PAD<123>	-1402	202.5	12	125
233	SEG_PAD<124>	-1426	202.5	12	125
234	SEG_PAD<125>	-1450	202.5	12	125
235	SEG_PAD<126>	-1474	202.5	12	125
236	SEG_PAD<127>	-1498	202.5	12	125
237	SEG_PAD<128>	-1522	202.5	12	125
238	COM_PAD<1>	-1626	202.5	12	125
239	COM_PAD<3>	-1650	202.5	12	125
240	COM_PAD<5>	-1674	202.5	12	125
241	COM_PAD<7>	-1698	202.5	12	125
242	COM_PAD<9>	-1722	202.5	12	125
243	COM_PAD<11>	-1746	202.5	12	125
244	COM_PAD<13>	-1770	202.5	12	125
245	COM_PAD<15>	-1794	202.5	12	125
246	COM_PAD<17>	-1818	202.5	12	125
247	COM_PAD<19>	-1842	202.5	12	125
248	COM_PAD<21>	-1866	202.5	12	125
249	COM_PAD<23>	-1890	202.5	12	125
250	COM_PAD<25>	-1914	202.5	12	125
251	COM_PAD<27>	-1938	202.5	12	125
252	COM_PAD<29>	-1962	202.5	12	125
253	COM_PAD<31>	-1986	202.5	12	125
254	COM_PAD<33>	-2010	202.5	12	125
255	COM_PAD<35>	-2034	202.5	12	125
256	DUMMY1	-2058	202.5	12	125

TRAY INFORMATION



REVISION HISTORY

Revision	Contents	Date
0.6	(First Release)	Nov. 20, 2014
0.7	One more Part Number is provided for Bump Height 15uM gold bumped die.	Feb. 5, 2015
0.8	Partial Display related contents are removed. Vlcd range is updated: 2.8V~5.467V → 2.83V~5.51V DC Characteristics table, Power Consumption table, and AC Characteristics table are updated.	Apr. 10, 2015
1.0	(Same as Revision 0.8)	Apr. 20, 2015
1.01	One more column, V_D, is added to the V_{LCD} Quick Reference table.	Apr. 8, 2016
1.02	The description of the CD pin when not used in S9 mode, is enforced: connect to Vdd or Vss.	Apr. 20, 2016