AiP31567A
132 SEG/65 COM Dot Matrix LCD Controller/Driver

Product Specification

Specification Revision History：

Version	Date	Description
2019-12-A1	2019-12	New

1、General Description

AiP31567A is a single-chip dot matrix LCD driver which incorporates LCD controller and common/segment drivers. AiP31567A can be connected directly to a microprocessor with 8-bit parallel interface, 4-line serial interface (SPI-4), 3-line serial interface (SPI-3) or I2C serial interface. Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 132×65 bits. The display data bits which are stored in DDRAM are directly related to the pixels of LCD panel. AiP31567A contains 132 segment-outputs, 64 common-outputs and 1 icon-common-output. With built-in oscillation circuit and low power consumption power circuit, AiP31567A generates LCD driving signal without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

Features:

- Single-chip LCD Controller & Driver
- On-chip Display Data RAM (DDRAM)
  - Capacity: 132×65=8580 bits
  - Directly display RAM pattern from DDRAM
- Selectable Display Duty (by SEL2 & SEL1)
  - 1/65 duty: 132 segment ×65 common
  - 1/55 duty: 132 segment ×55 common
  - 1/49 duty: 132 segment ×49 common
  - 1/33 duty: 132 segment ×33 common
- Microprocessor Interface
  - Bidirectional 8-bit parallel interface supports:8080-series and 6800-series MPU
  - Serial interface: 4-line SPI (SPI-4), 3-line SPI (SPI-3), I2C
- Abundant Functions
  - Display ON/OFF, Normal/Reverse Display Mode, Set Display Start Line, Read IC Status, Set all Display Points ON, Set LCD Bias, Electronic Volume Control, Read-modify-Write, Select Segment Driver Direction, Power Saving Mode, Select Common Driver Direction, Select Voltage Regulator Resistor Ratio (for V0).
- External Hardware Reset Pin (RSTB)
- Built-in Oscillation Circuit
  - No external component required
- Low Power Consumption Analog Circuit
  - Voltage Booster (4X, 5X)
  - High-accuracy Voltage Regulator for LCD Vop: (Thermal Gradient: -0.05%/℃)
  - Voltage Follower for LCD Bias Voltage
- Wide Operation Voltage Range
  - VDD1-GND1=1.8V~3.3V (TYP.)
  - VDD2-GND2=1.8V~3.3V (TYP.)
  - VDD3-GND3=1.8V~3.3V (TYP.)
- Temperature Range: -40℃~85℃
- Package Type: COG

2、Block Diagram And Pin Description

2.1、Block Diagram

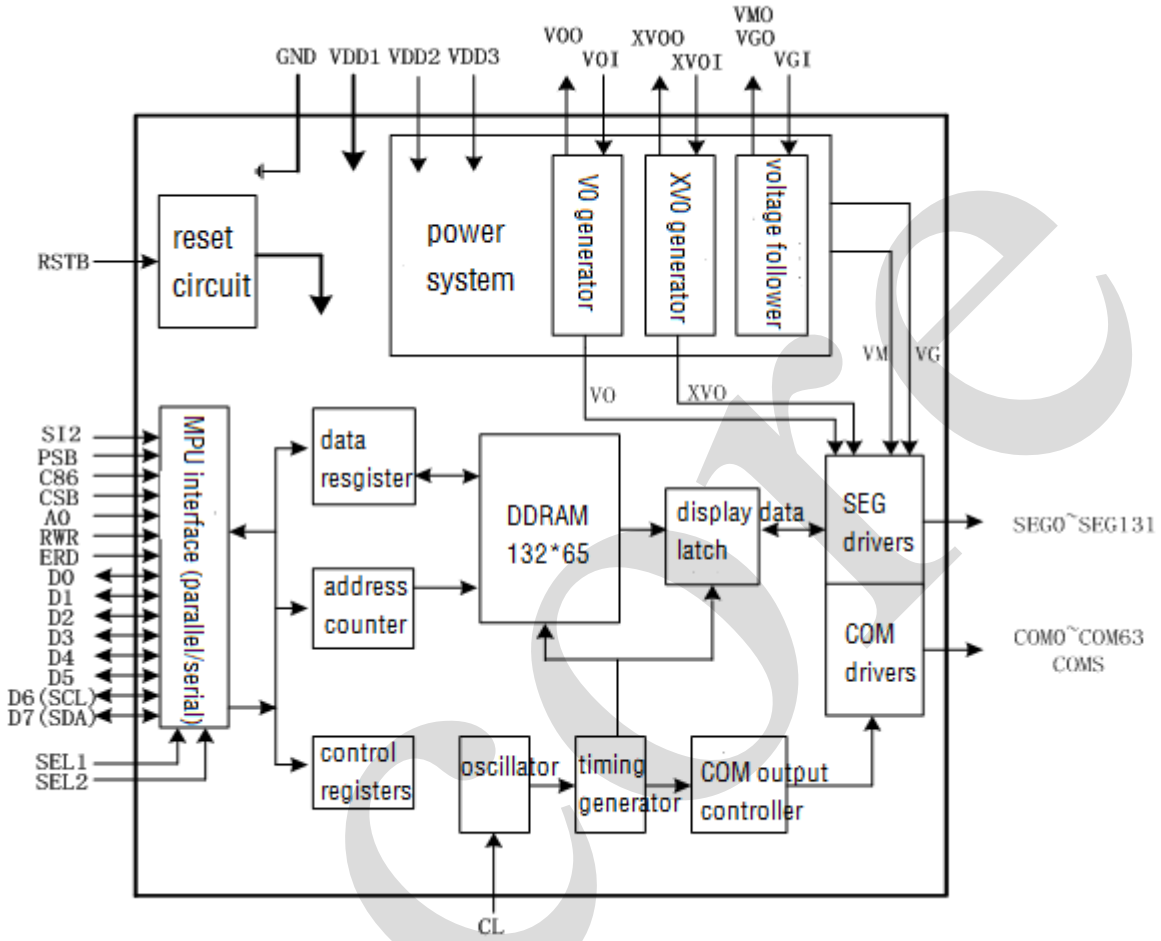


Figure 1. Functional diagram

2.2、Pin Description

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">LCD Driver Output Pins</td></tr>
<tr><td>104~235</td><td>SEG0 to SEG131</td><td>O</td><td>LCD segment driver outputs.
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Inverse display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>GND</td></tr>
<tr><td>H</td><td>-</td><td>GND</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>GND</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>GND</td></tr>
<tr><td colspan="2">display OFF, power save</td><td>GND</td><td>GND</td></tr>
</table></td></tr>
<tr><td>71~102, 236~267</td><td>COM0 to COM63</td><td>O</td><td>LCD common driver outputs.
The internal scanning signal and the frame control the output voltage.
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Comment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Inverse display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">display OFF, power save</td><td colspan="2">GND</td></tr>
</table></td></tr>
<tr><td>103, 268</td><td>COMS1, COMS2 (COMS)</td><td>O</td><td>LCD common driver outputs for icons.
The output signals of these two pins are the same.
When icon feature is not used, these pins should be left open.</td></tr>
<tr><td colspan="4">Microprocessor Interface Pins</td></tr>
<tr><td>4</td><td>RSTB</td><td>I</td><td>Hardware reset input pin. When RSTB is “L”, internal initialization is executed and the internal registers will be initialized.</td></tr>
<tr><td>2</td><td>CSB</td><td>I</td><td>Chip select input pin. Interface access is enabled when CSB is “L”. When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>5</td><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0=“H”: Indicates that signals on D[7:0] are display data.
A0=“L”: Indicates that signals on D[7:0] are command.</td></tr>
<tr><td>6</td><td>RWR</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”,
<table>
<tr><th>C86</th><th>MPU type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is used to decide slave address (SA1) in I2C serial interface. RWR is not used in 3-line and 4-line SPI interface and should fix to “H” by VDD1 or VDDH.</td></tr>
</table>

<table>
<tr><td>7</td><td>ERD</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”,
<table>
<tr><th>C86</th><th>MPU type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=“H”: When E is “H”, D[7:0] are in output mode.
R/W=“L”: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table>
ERD is used to decide slave address (SA0) in I2C serial interface.
ERD is not used in 3-Line and 4-Line SPI interface and should fix to “H” by VDD1 or VDDH.</td></tr>
<tr><td rowspan="2">9~15, 17</td><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: (6800 or 8080 mode):
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface: 4-line SPI, 3-line SPI or I2C serial interface:
D[0]=SCL: Serial clock input.
D[1]=SDA_IN: Serial data input.
D[2:3]=SDA_OUT: Serial data output.
D[1:3] must be connected together as SDA.:
D[4:7]=(1,1,1,1): ID Pin. D[4:7] should fix to “H” or “L” by VDDH or GNDL. ID[0:3] can be read 4-bit ID only for serial interface from D[4:7].</td></tr>
<tr><td colspan="4">Configuration Pins</td></tr>
<tr><td>3, 8</td><td>VDD</td><td>O</td><td>Logic “1” level for option pins which should connected to “H”.</td></tr>
<tr><td>16, 56, 62, 66</td><td>GND</td><td>O</td><td>Logic “0” level for option pins which should connected to “L”.</td></tr>
<tr><td>61</td><td>PSB</td><td>I</td><td>PSB selects the interface type: Serial or Parallel.</td></tr>
<tr><td>59</td><td>C86</td><td>I</td><td>C86 selects the microprocessor type in parallel interface mode</td></tr>
<tr><td>63</td><td>SI2</td><td>I</td><td>SI2 selects the interface type: I2C serial interface or not
<table>
<tr><th>SI2</th><th>PSB</th><th>C86</th><th>Selected Interface</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Serial 3-Line SPI Interface</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Serial 4-Line SPI Interface</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Parallel 8080 Series MPU Interface</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Parallel 6800 Series MPU Interface</td></tr>
<tr><td>H</td><td>L</td><td>X</td><td>I2C Serial Interface</td></tr>
</table></td></tr>
<tr><td>65, 67</td><td>SEL[2:1]</td><td>I</td><td>These pins select the display duty and bias of AiP31567A.
<table>
<tr><th>SEL2</th><th>SEL1</th><th>Duty</th><th>Bias</th></tr>
<tr><td>L</td><td>L</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>H</td><td>L</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>H</td><td>H</td><td>1/55</td><td>1/8 or 1/6</td></tr>
</table></td></tr>
<tr><td>58</td><td>TSEL</td><td>I</td><td>TSEL is high power mode function.
TSEL=“L”, Off mode (1.6V≤VG<VDD2-0.2V, for general use).</td></tr>
</table>

			TSEL="H", On mode (VDD2-0.2V≤VG<3.8V). Note: VG=(Vop/bias)×2
Power System Pins			
18, 19, 68	VDD1	power	Digital power. If VDD1=VDD2, connect to VDD2 externally.
20~22, 69	VDD2	power	Analog power. If VDD1=VDD2, connect to VDD1 externally.
23, 70	VDD3	power	Power for reference voltage circuit.
24, 25	GND1	power	Digital ground. Connect to GND2 externally.
27~29	GND2	power	Analog ground. Connect to GND1 externally.
26	GND3	power	Ground for reference voltage circuit.
33, 34, 30~32	V0O V0I	power	V0 is the LCD driving voltage for common circuits at negative frame. V0O is the output of V0 regulator. V0I is the V0 input of common circuits. Be sure that: V0≥VG>VM>GND≥XV0 (under operation). V0O, V0I should be connected together in ITO layout.
35, 36, 37~39	XV0O XV0I	power	XV0 is the LCD driving voltage for common circuits at positive frame. XV0O is the output of XV0 regulator. XV0I is the XV0 input of common circuits. XV0O, XV0I should be connected together in ITO layout.
45, 42~44	VGO VGI	power	VG is the LCD driving voltage for segment circuits. VGO is the output of VG regulator. VGI is the VG input of segment circuits. VGO, VGI should be connected together in ITO layout.
40, 41	VMO	power	VM is the LCD driving voltage for common circuits. 0.8V≤VM<VG.
Test Pins			
55	VREF	T	Test pin for power system. This pin must be left open (without any kinds of connection).
50~54, 46~47	T1~T8	T	Do NOT use. Reserved for testing. Must be floating.
49	TFCOM	T	Do NOT use. Reserved for testing. Must be floating.
1	CL	T	Do not use. Reserved for testing. Must be floating.

Note: After VDD1 is turned ON, any MPU interface pins cannot be left floating.

2.3、Recommend ITO Resistance

Pin Name	ITO Resistance
VMO, VREF, T[1:8], TFCOM, CL	floating
VDD1,VDD2,VDD3	<100Ω
GND1，GND2，GND3	<70Ω
V0(V0I, V0O), VG(VGI, VGO), XV0(XV0O, XV0I)	<200Ω
A0, RWR, ERD, CSB, D[7:0]	<700Ω
PSB, C86, SEL[2:1]，SI2，TSEL	<5kΩ
D[0:3] (I2C)	<100Ω
D[0:3] (SPI)	<300Ω
RSTB	2~3kΩ

Note:

[1] To prevent the ESD pulse resetting the internal register, applications should increase the resistance of RSTB signal (add a series resistor or increase ITO resistance). The value is different from modules.

[2] The option setting to be “H” should connect to VDD1 or VDDH.

[3] The option setting to be “L” should connect to GND.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
digital power supply voltage	VDD1	-	-0.3	4.0	V
analog power supply voltage	VDD2, VDD3	-	-0.3	4.0	V
LCD power supply voltage	V0-XV0	-	-0.3	18	V
input voltage	VIN	-	-0.3	VDD1+0.3	V
operating temperature	T_{OPR}	-	-40	+85	℃
storage temperature	T_{stg}	-	-55	+125	℃

Note:

[1] Insure the voltage levels of V0, VDD2, VG, VM, GND and XV0 always match the correct relation: V0≥VDD2>VG>VM>GND≥XV0

[2] VIN should be less than or equal to 3.6V. (VIN≤3.6V)

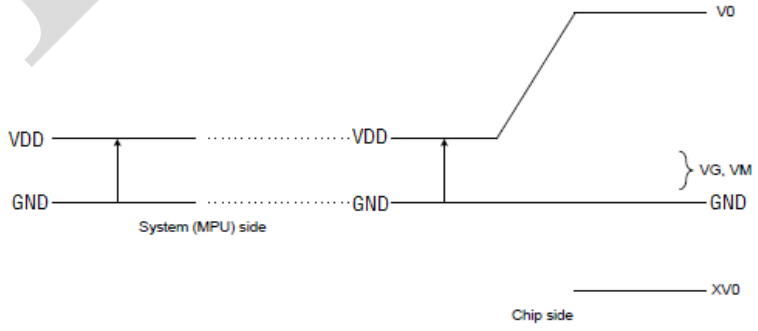


Figure 2. Voltage relationship

3.2、Electrical Characteristics (DC Characteristics)

3.2.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable Pin
Operating Voltage (1)	VDD1	-	1.7	-	3.6	V	VDD1
Operating Voltage (2)	VDD2	-	1.7	-	3.6	V	VDD2
Operating Voltage (3)	VDD3	-	1.7	-	3.6	V	VDD3
Input High-level Voltage	V_{IHC}	-	0.7× VDD1	-	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}	-	GND1	-	0.3× VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA,VDD1=1.8V	0.8× VDD1	-	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA,VDD1=1.8V	GND1	-	0.2× VDD1	V	D[7:0]
Input Leakage Current	I_{LI}	-	-1.0	-	1.0	uA	MPU Interface
Output Leakage Current	I_{LO}	-	-3.0	-	3.0	uA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	T_{amb}=25℃, VOP=8.5V, ΔV=0.85V	-	0.6	0.8	kΩ	COMx
		T_{amb}=25℃, VG=1.9V, ΔV=0.19V	-	1.3	1.5	kΩ	SEGx
Frame Frequency	FR	Duty=1/65, OP=8.5V, T_{amb}=25℃	70	75	80	Hz	-
LCD Power Supply Voltage	VLCD	T_{amb}=25℃	4.0	-	13.65	V	V0-XV0

3.2.2、DC Characteristics 2

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Display Pattern: Black (Static)	ISS	VDD1=VDD2=VDD3=3.0V, Booster X5 VOP=8.5V, Bias=1/9 T_{amb}=25℃	-	80	130	uA
Display OFF	ISS	VDD1=VDD2=VDD3=3.0V, Booster X5 VOP=8.5V, Bias=1/9, T_{amb}=25℃	-	70	110	uA
Power Down	ISS	VDD1=VDD2=VDD3=3.0V, T_{amb}=25℃	-	1.0	3.0	uA

Note: Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

3.3、Electrical Characteristics (AC Characteristics)

3.3.1、System Bus Timing for 6800 Series MPU

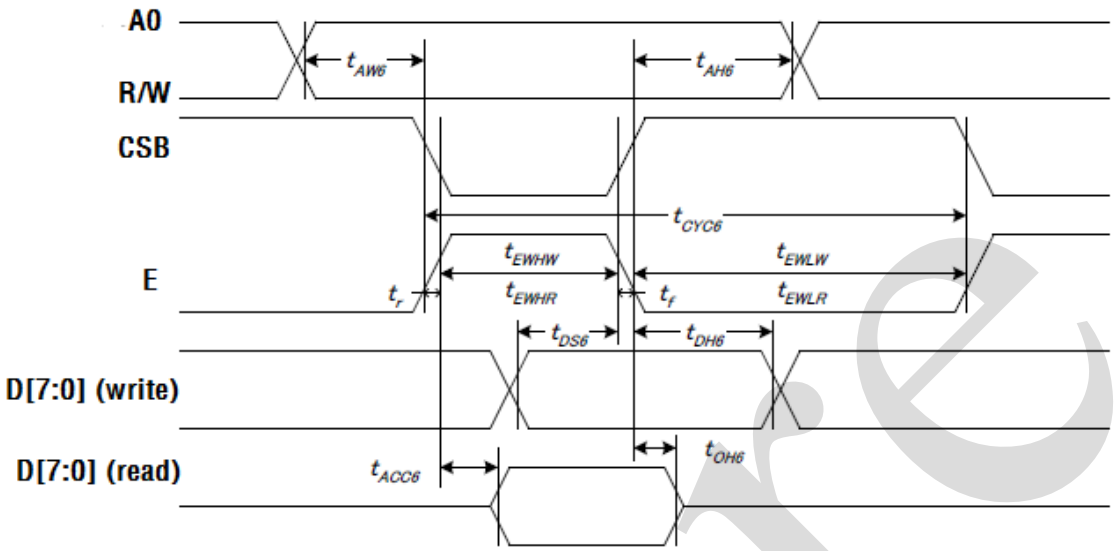


Figure 3. AC Characteristics 1

(VDD1=3.3V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
address setup time	A0	t_{AW6}	-	0	-	ns
address hold time		t_{AH6}	-	10	-	ns
system cycle time	E	t_{CYC6}	-	240	-	ns
enable L pulse width (WRITE)		t_{EWLW}	-	80	-	ns
enable H pulse width (WRITE)		t_{EWHW}	-	80	-	ns
enable L pulse width (READ)		t_{EWLR}	-	80	-	ns
enable H pulse width (READ)		t_{EWHR}	-	140	-	ns
write data setup time	D[7:0]	t_{DS6}	-	40	-	ns
write data hold time		t_{DH6}	-	10	-	ns
read data access time		t_{ACC6}	CL=16pF	-	70	ns
read data output disable time		t_{OH6}	CL=16pF	5	50	ns

(VDD1=2.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
address setup time	A0	t_{AW6}	-	0	-	ns
address hold time		t_{AH6}	-	0	-	ns
system cycle time	E	t_{CYC6}	-	400	-	ns
enable L pulse width (WRITE)		t_{EWLW}	-	220	-	ns
enable H pulse width (WRITE)		t_{EWHW}	-	180	-	ns
enable L pulse width (READ)		t_{EWLR}	-	220	-	ns
enable H pulse width (READ)		t_{EWHR}	-	180	-	ns
write data setup time	D[7:0]	t_{DS6}	-	40	-	ns
write data hold time		t_{DH6}	-	20	-	ns
read data access time		t_{ACC6}	CL=16pF	-	140	ns
read data output disable time		t_{OH6}	CL=16pF	10	100	ns

(VDD1=1.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
address setup time	A0	t_{AW6}	-	0	-	ns
address hold time		t_{AH6}	-	0	-	ns
system cycle time	E	t_{CYC6}	-	640	-	ns
enable L pulse width (WRITE)		t_{EWLW}	-	360	-	ns
enable H pulse width (WRITE)		t_{EWHW}	-	280	-	ns
enable L pulse width (READ)		t_{EWLR}	-	360	-	ns
enable H pulse width (READ)		t_{EWHR}	-	280	-	ns
write data setup time	D[7:0]	t_{DS6}	-	80	-	ns
write data hold time		t_{DH6}	-	20	-	ns
read data access time		t_{ACC6}	CL=16pF	-	240	ns
read data output disable time		t_{OH6}	CL=16pF	10	200	ns

Note:

[1] The input signal rise time and fall time (tr, tf) is specified at 15ns or less. When the system cycle time is extremely fast, $(tr+tf) \leq (t_{CYC6}-t_{EWLW}-t_{EWHW})$ for $(tr+tf) \leq (t_{CYC6}-t_{EWLR}-t_{EWHR})$ are specified.

[2] All timing is specified using 20% and 80% of VDD1 as the reference.

[3] t_{EWLW} and t_{EWLR} are specified as the overlap between CSB being "L" and E.

3.3.2、System Bus Timing for 8080 Series MPU

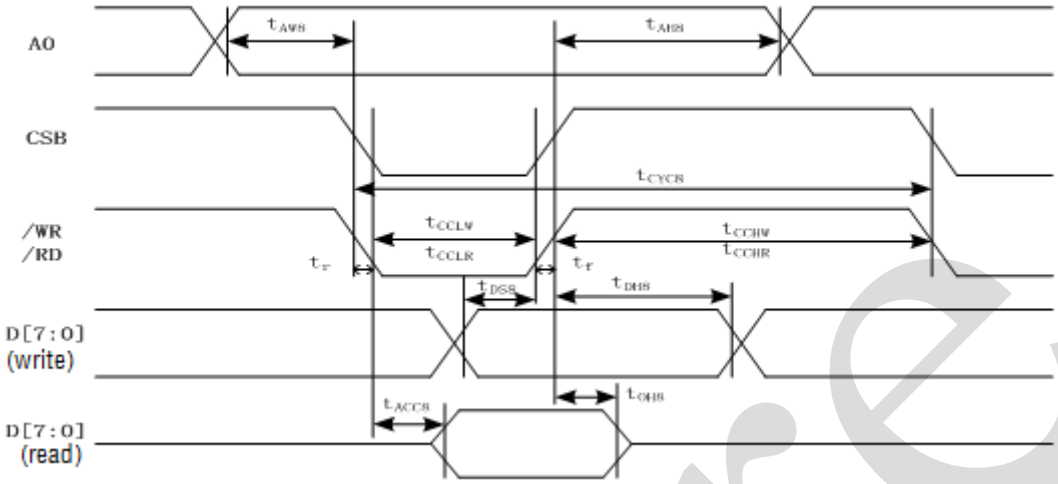


Figure 4. AC Characteristics 2

(VDD1=3.3V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
address setup time	A0	t_{AW8}	-	0	-	ns
address hold time		t_{AH8}	-	10	-	ns
system cycle time	/WR	t_{CYC8}	-	240	-	ns
/WR L pulse width (WRITE)		t_{CCLW}	-	80	-	ns
/WR H pulse width (WRITE)		t_{CCHW}	-	80	-	ns
/RD L pulse width (READ)	RD	t_{CCLR}	-	140	-	ns
/RD H pulse width (READ)		t_{CCHR}	-	80	-	ns
write data setup time	D[7:0]	t_{DS8}	-	40	-	ns
write data hold time		t_{DH8}	-	20	-	ns
read access time		t_{ACC8}	CL=16pF	-	70	ns
read output disable time		t_{OH8}	CL=16pF	5	50	ns

(VDD1=2.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
address setup time	A0	t_{AW8}	-	0	-	ns
address hold time		t_{AH8}	-	0	-	ns
system cycle time	/WR	t_{CYC8}	-	400	-	ns
/WR L pulse width (WRITE)		t_{CCLW}	-	220	-	ns
/WR H pulse width (WRITE)		t_{CCHW}	-	180	-	ns
/RD L pulse width (READ)	RD	t_{CCLR}	-	220	-	ns
/RD H pulse width (READ)		t_{CCHR}	-	180	-	ns
write data setup time	D[7:0]	t_{DS8}	-	40	-	ns
write data hold time		t_{DH8}	-	20	-	ns
read access time		t_{ACC8}	CL=16pF	-	140	ns
read output disable time		t_{OH8}	CL=16pF	10	100	ns

(VDD1=1.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
address setup time	A0	t_{AW8}	-	0	-	ns
address hold time		t_{AH8}	-	0	-	ns
system cycle time	/WR	t_{CYC8}	-	640	-	ns
/WR L pulse width (WRITE)		t_{CCLW}	-	360	-	ns
/WR H pulse width (WRITE)		t_{CCHW}	-	280	-	ns
/RD L pulse width (READ)	RD	t_{CCLR}	-	360	-	ns
/RD H pulse width (READ)		t_{CCHR}	-	280	-	ns
write data setup time	D[7:0]	t_{DS8}	-	80	-	ns
write data hold time		t_{DH8}	-	20	-	ns
read access time		t_{ACC8}	CL=16pF	-	240	ns
read output disable time		t_{OH8}	CL=16pF	10	200	ns

Note:

[1] The input signal rise time and fall time (tr, tf) is specified at 15ns or less. When the system cycle time is extremely fast, $(tr+tf) \leq (t_{CYC8}-t_{CCLW}-t_{CCHW})$ for $(tr+tf) \leq (t_{CYC8}-t_{CCLR}-t_{CCHR})$ are specified.

[2] All timing is specified using 20% and 80% of VDD1 as the reference.

[3] t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.

3.3.3、System Bus Timing for 4-Line Serial Interface

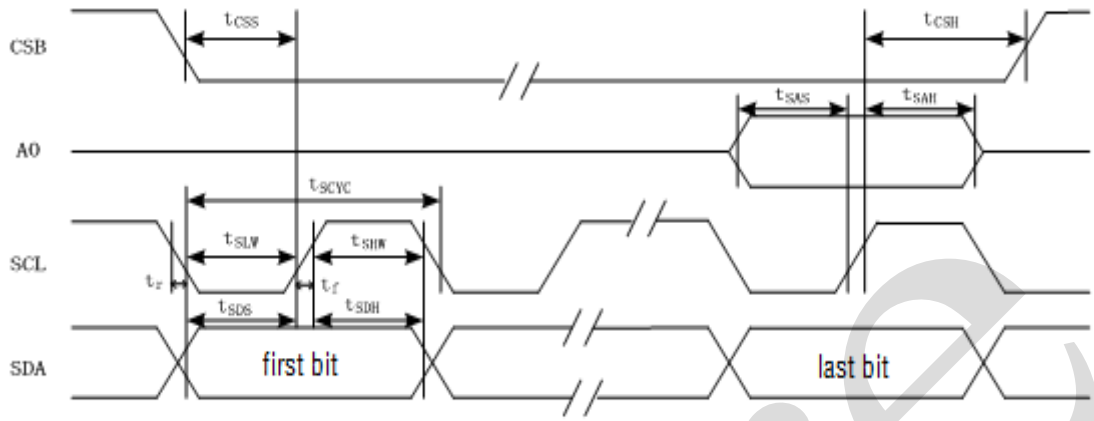


Figure 5. AC Characteristics 3

(VDD1=3.3V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
serial clock period	SCL	t_{SCYC}	-	50	-	ns
SCL “H” pulse width		t_{SHW}	-	25	-	ns
SCL “L” pulse width		t_{SLW}	-	25	-	ns
address setup time	A0	t_{SAS}	-	20	-	ns
address hold time		t_{SAH}	-	10	-	ns
data setup time	SDA	t_{SDS}	-	20	-	ns
data hold time		t_{SDH}	-	10	-	ns
CSB-SCL time	CSB	t_{CSS}	-	20	-	ns
CSB-SCL time		t_{CSH}	-	40	-	ns

(VDD1=2.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
serial clock period	SCL	t_{SCYC}	-	100	-	ns
SCL “H” pulse width		t_{SHW}	-	50	-	ns
SCL “L” pulse width		t_{SLW}	-	50	-	ns
address setup time	A0	t_{SAS}	-	30	-	ns
address hold time		t_{SAH}	-	20	-	ns
data setup time	SDA	t_{SDS}	-	30	-	ns
data hold time		t_{SDH}	-	20	-	ns
CSB-SCL time	CSB	t_{CSS}	-	30	-	ns
CSB-SCL time		t_{CSH}	-	60	-	ns

(VDD1=1.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
serial clock period	SCL	t_{SCYC}	-	200	-	ns
SCL “H” pulse width		t_{SHW}	-	80	-	ns
SCL “L” pulse width		t_{SLW}	-	80	-	ns
address setup time	A0	t_{SAS}	-	60	-	ns
address hold time		t_{SAH}	-	30	-	ns
data setup time	SDA	t_{SDS}	-	60	-	ns
data hold time		t_{SDH}	-	30	-	ns
CSB-SCL time	CSB	t_{CSS}	-	40	-	ns
CSB-SCL time		t_{CSH}	-	100	-	ns

Note:

[1] The input signal rise and fall time (tr, tf) are specified at 15ns or less.

[2] All timing is specified using 20% and 80% of VDD1 as the standard.

3.3.4、System Bus Timing for 3-Line Serial Interface

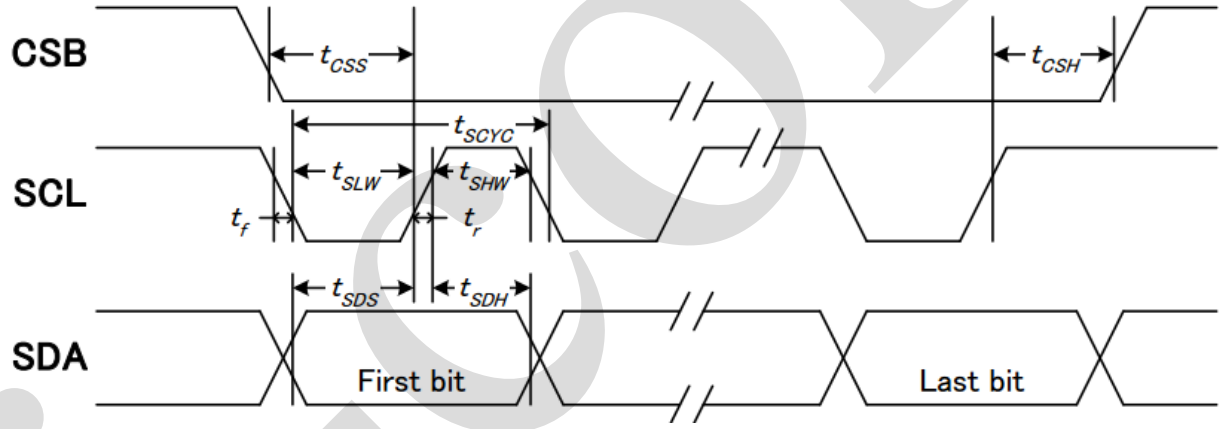


Figure 6. AC Characteristics 4

(VDD1=3.3V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
serial clock period	SCL	t_{SCYC}	-	50	-	ns
SCL “H” pulse width		t_{SHW}	-	25	-	ns
SCL “L” pulse width		t_{SLW}	-	25	-	ns
data setup time	SDA	t_{SDS}	-	20	-	ns
data hold time		t_{SDH}	-	10	-	ns
CSB-SCL time	CSB	t_{CSS}	-	20	-	ns
CSB-SCL time		t_{CSH}	-	40	-	ns

(VDD1=2.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
serial clock period	SCL	t_{SCYC}	-	100	-	ns
SCL “H” pulse width		t_{SHW}	-	50	-	ns
SCL “L” pulse width		t_{SLW}	-	50	-	ns
data setup time	SDA	t_{SDS}	-	30	-	ns
data hold time		t_{SDH}	-	20	-	ns
CSB-SCL time	CSB	t_{CSS}	-	30	-	ns
CSB-SCL time		t_{CSH}	-	60	-	ns

(VDD1=1.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
serial clock period	SCL	t_{SCYC}	-	200	-	ns
SCL “H” pulse width		t_{SHW}	-	80	-	ns
SCL “L” pulse width		t_{SLW}	-	80	-	ns
data setup time	SDA	t_{SDS}	-	60	-	ns
data hold time		t_{SDH}	-	30	-	ns
CSB-SCL time	CSB	t_{CSS}	-	40	-	ns
CSB-SCL time		t_{CSH}	-	100	-	ns

3.3.5、Serial Interface (I2C Interface)

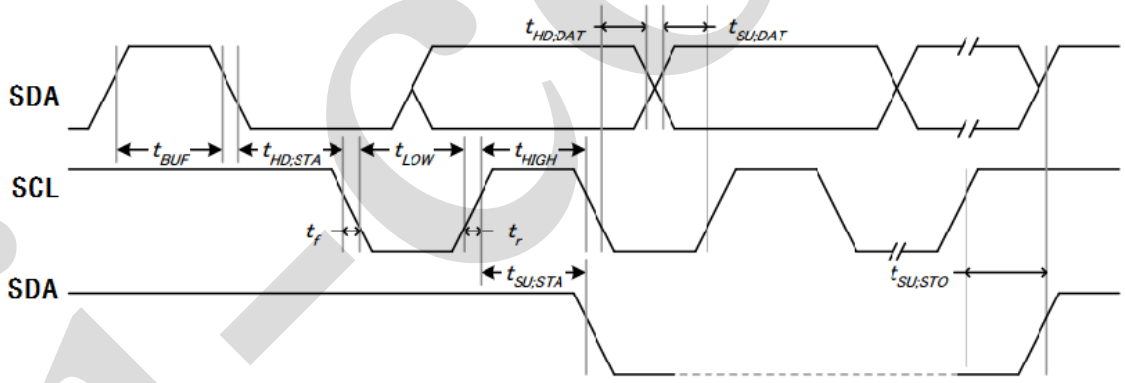


Figure 7. AC Characteristics 5

(VDD1=3.3V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
SCL clock frequency	SCL	f_{SCL}	-	-	400	kHz
SCL clock low period		t_{LOW}	-	160	-	ns
SCL clock high period		t_{HIGH}	-	60	-	ns
data set-up time	SDA	$t_{SU;DATA}$	-	80	-	ns
data hold time		$t_{HD;DATA}$	-	40	-	ns
setup time for a repeated START condition		$t_{SU;STA}$	-	90	-	ns

start condition hold time		$t_{HD;STA}$	-	220	-	ns
setup time for STOP condition		$t_{SU;STO}$	-	110	-	ns
bus free time between a STOP and START		t_{BUF}	-	150	-	ns

(VDD1=2.8V, T_{amb}=25℃)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
SCL clock frequency	SCL	f_{SCL}	-	-	400	kHz
SCL clock low period		t_{LOW}	-	160	-	ns
SCL clock high period		t_{HIGH}	-	60	-	ns
data set-up time	SDA	$t_{SU;DATA}$	-	80	-	ns
data hold time		$t_{HD;DATA}$	-	40	-	ns
setup time for a repeated START condition		$t_{SU;STA}$	-	90	-	ns
start condition hold time		$t_{HD;STA}$	-	220	-	ns
setup time for STOP condition		$t_{SU;STO}$	-	110	-	ns
bus free time between a STOP and START		t_{BUF}	-	150	-	ns

3.3.6、Hardware Reset Timing

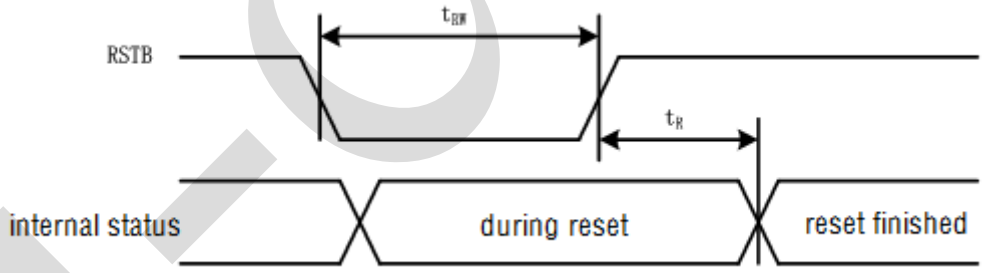


Figure 8. AC Characteristics 6

(VDD1=3.3V, T_{amb}=25℃)

Item	Symbol	Conditions	Min.	Max.	Unit
reset time	t_R	VDD1=3.3V	-	1.0	us
		VDD1=2.8V	-	2.0	us
		VDD1=1.8V	-	3.0	us
reset “L” pulse width	t_{RW}	VDD1=3.3V	1.0	-	us
		VDD1=2.8V	2.0	-	us
		VDD1=1.8V	3.0	-	us

4、Function Description

4.1、Microprocessor Interface

4.1.1、Chip Select Input

CSB pin is used for chip selection. When CSB is “L”, the microprocessor interface is enabled and AiP31567A can interface with an MPU. When CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In the serial interface (3-Line, 4-Line SPI and I2C), the internal shift register and serial counter are reset when CSB is “H”.

4.1.2、Interface Selection

The interface selection is controlled by C86, PSB and SI2 pins. The selection for parallel or serial interface is shown in the following table:

SI2	PSB	C86	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
L	L	L	CSB	-	-	-	refer to serial interface	3-Line SPI interface
L	L	H		A0	-	-		4-Line SPI interface
L	H	L			/RD	/WR	D[7:0]	8080-series parallel interface
L	H	H			E	R/W		6800-series parallel interface
H	L	X	-	-	SA0	SA1	refer to serial interface	I2C serial interface

Note: The un-used pins are marked as “-” and should be fixed to “H” by VDD1 or VDDH.

4.1.3、Parallel Interface

The data transfer type is determined by signals on A0, ERD and RWR as shown in the following table.

Common Pins		6800-Series		8080-Series		Description
CSB	A0	E(ERD)	R/W(RWR)	/RD(ERD)	/WR(RWR)	
L	H	H	H	L	H	display data read out
	H	H	L	H	L	display data write
	L	H	H	L	H	internal status read
	L	H	L	H	L	writes to internal register (instruction)

4.1.4、Setting Serial Interface

Serial Mode	SI2	PSB	C86	CSB	A0	ERD	RWR	D[7:0]
3-Line SPI interface	L	L	L	CSB	-	-	-	ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL
4-Line SPI interface	L	L	H	CSB	A0	-	-	ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL
I2C serial interface	H	L	X	-	-	SA0	SA1	ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL

Note:

[1] The un-used pins are marked as “-” and should be fixed to “H” by VDD1 or VDDH.

[2] C86 is marked as “X” and can be fixed to “H” or “L”.

4.2、4-line SPI interface (SI2="L", PSB="L" and C86="H")

WhenAiP31567A is active (CSB="L"), serial data (SDA) and serial clock (SCL) inputs are enabled. WhenAiP31567A is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCL. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is "H" and will be instruction when A0 is "L". The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCL signal quality is very important and external noise maybe causes unexpected data/instruction latch.

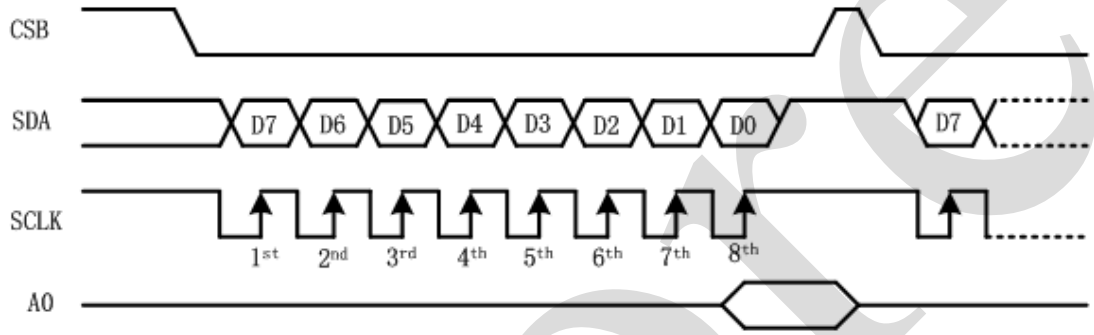


Figure 9. 4-Line SPI Access

Note: Some MPU will set the interface to be Hi-Z (high impedance) mode when power saving mode or after hardware reset. This is not allowed when the VDD1of AiP31567A is turned ON. Because the floating input (especially for those control pins such as CSB, RSTB, RWR or ERD…) maybe cause abnormal latch and cause abnormal display.

4.3、3-line SPI interface (SI2="L", PSB="L" and C86="L")

The 3-Line SPI (9-bit) uses 3 pins (CSB, SDA and SCL) to communicate with MPU. When CSB is "L", IC is active and the SDA and SCL pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9th) clock. After CSB returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit at the 1st bit of each 9-bit serial data.

4.3.1、Write Parameter by 3-Line SPI (A0=1)

When A0 is "1", the transferred 8-bit is parameter.

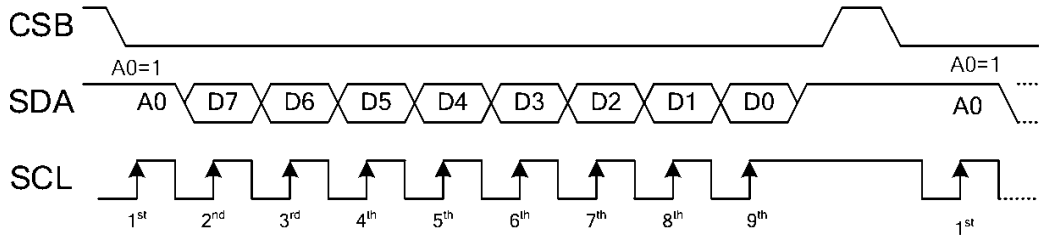


Figure 10. 3-Line SPI Write Data

4.3.2、Write Instruction by 3-Line SPI (A0=0)

When A0 is "0", the transferred 8-bit is instruction.

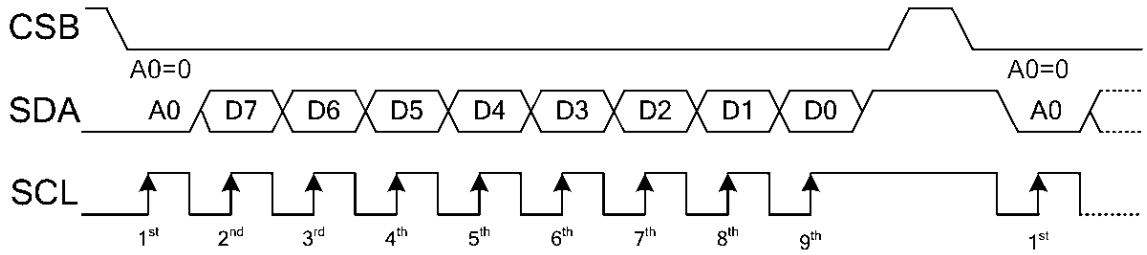


Figure 11. 3-Line SPI Write Instruction

4.4、I2C serial interface (SI2="H", PSB="L" and C86="X")

The I2C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

4.4.1、Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Figure 12.

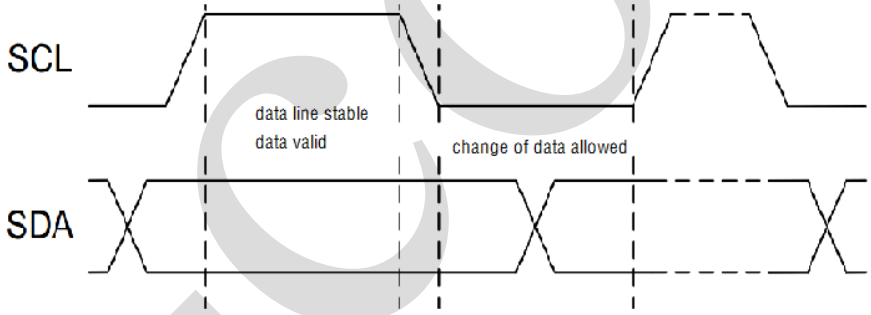


Figure 12. Bit Transfer

4.4.2、Start and Stop Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 13.

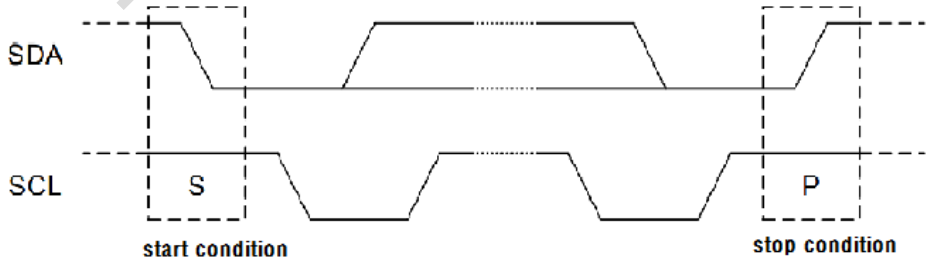


Figure 13. Definition of STRAT and STOP Condition

4.4.3、System Configuration

The system configuration is illustrated in Figure 14 and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

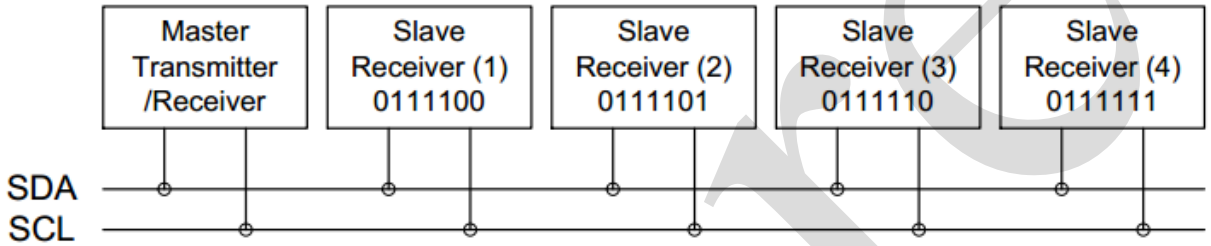


Figure 14. System Configuration

4.4.4、Acknowledgement

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I2C Interface is illustrated in Figure 15.

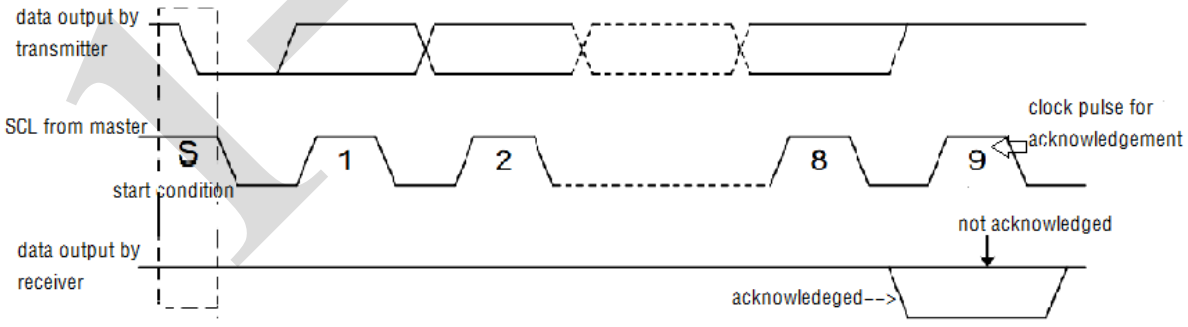
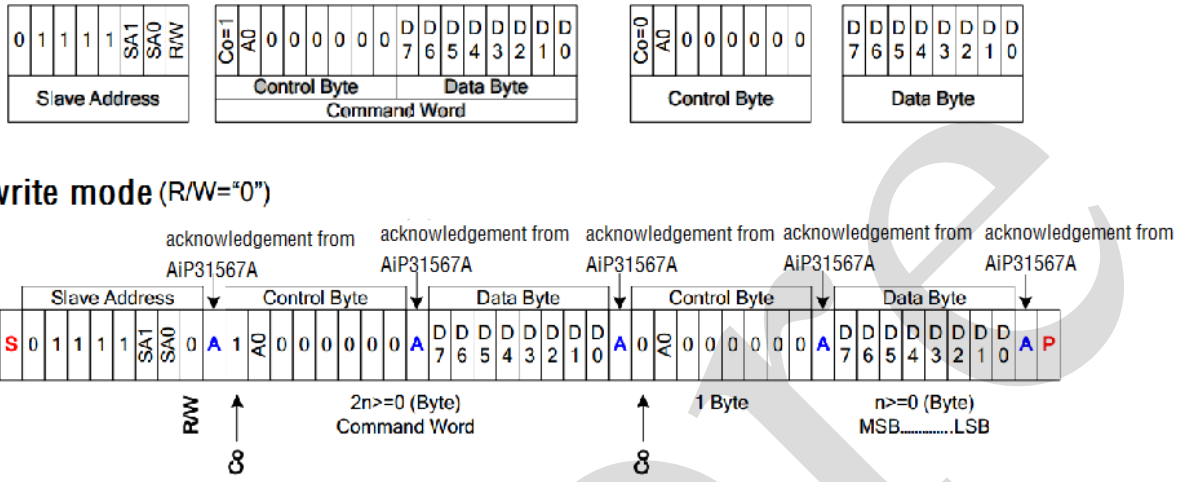


Figure 15. Acknowledgement of I2C Interface

4.4.5、I2C Interface Protocol

AiP31567A supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for AiP31567A. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (GND) or logic 1 (VDDH). The I2C Interface protocol is illustrated in Figure 16.



C_O	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

Figure 16. I2C Interface Protocol

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words are followed and define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended AiP31567A device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of AiP31567A will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

4.5、Data Transfer

AiP31567A uses bus latch and internal data bus for parallel interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Figure 17. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Figure 18. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

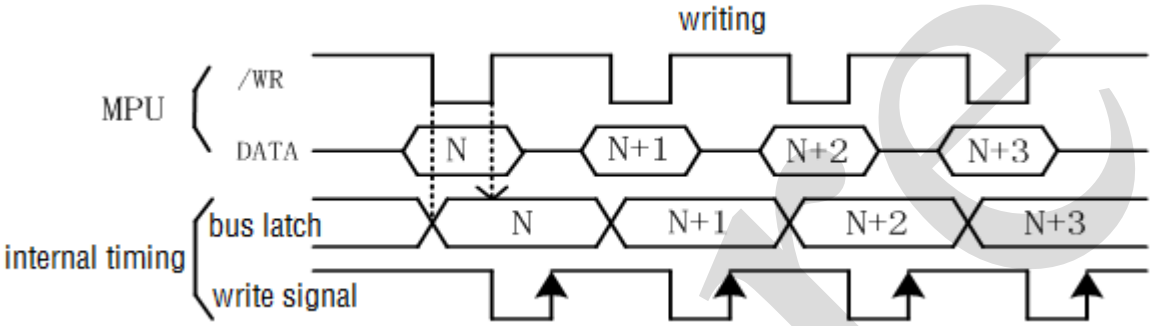


Figure 17. Data Transfer: Write

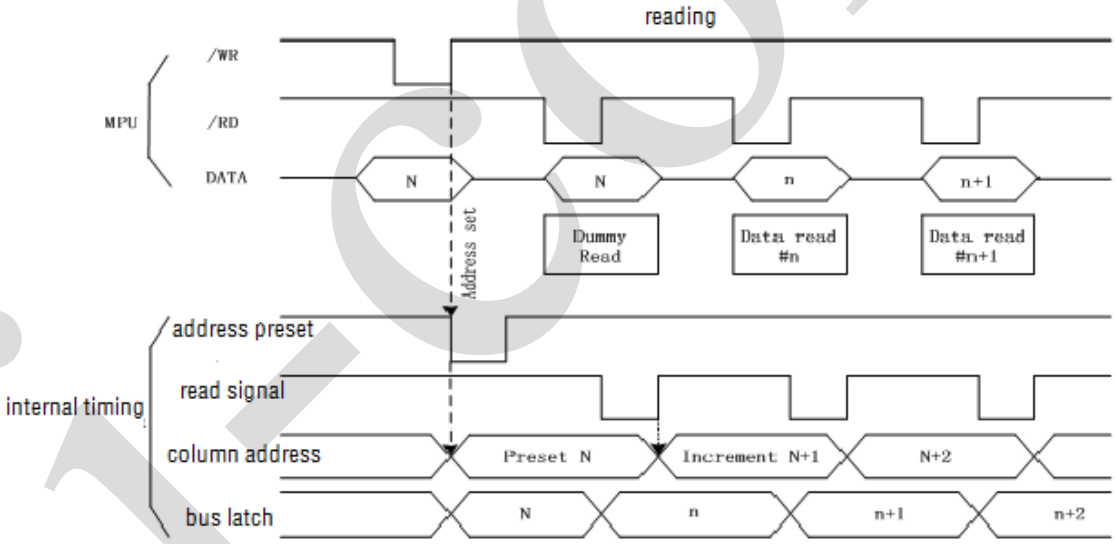


Figure 18. Data Transfer: Read

Note: 8080 interface: 8-bit;
6800 interface: 8-bit;
3-Line interface: 1-bit;
4-Line interface: 1-bit;
I2C interface: 8-bit.

4.6、Display Data Ram (DDRAM)

AiP31567A is built-in a RAM with 132×65 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Figure 19 detailed illustration). The rows are divided into: 8 pages (Page-0~Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0). Refer to Figure 20 for detailed illustration. The microprocessor can write to and read from DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

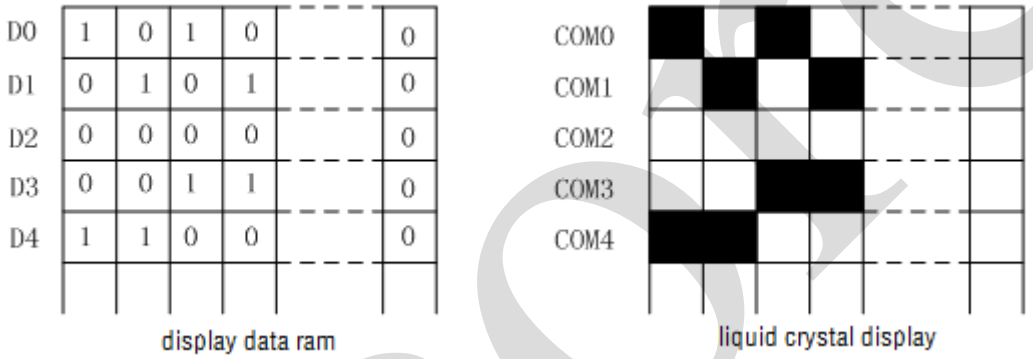


Figure 19. DDRAM Mapping (Default Setting)

Figure 20. DDRAM Format

4.7、Addressing

Data is downloaded into the Display Data RAM matrix in AiP31567A as byte-format. The Display Data RAM has a matrix of 132 by 65 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

4.7.1、Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the “Page Address Set” instruction only. The Page Address must be set before accessing DDRAM content. Page Address “8” is a special RAM area for the icons with only one valid bit: D0.

4.7.2、Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “83h”) because the Column Address and Page Address circuits are independent. For example, both Page Address and Column Address should be assigned for changing the DDRAM pointer from (Page-0, Column-83h) to (Page-1, Column-0).

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG). It is necessary to rewrite the display data into DDRAM after changing MX setting.

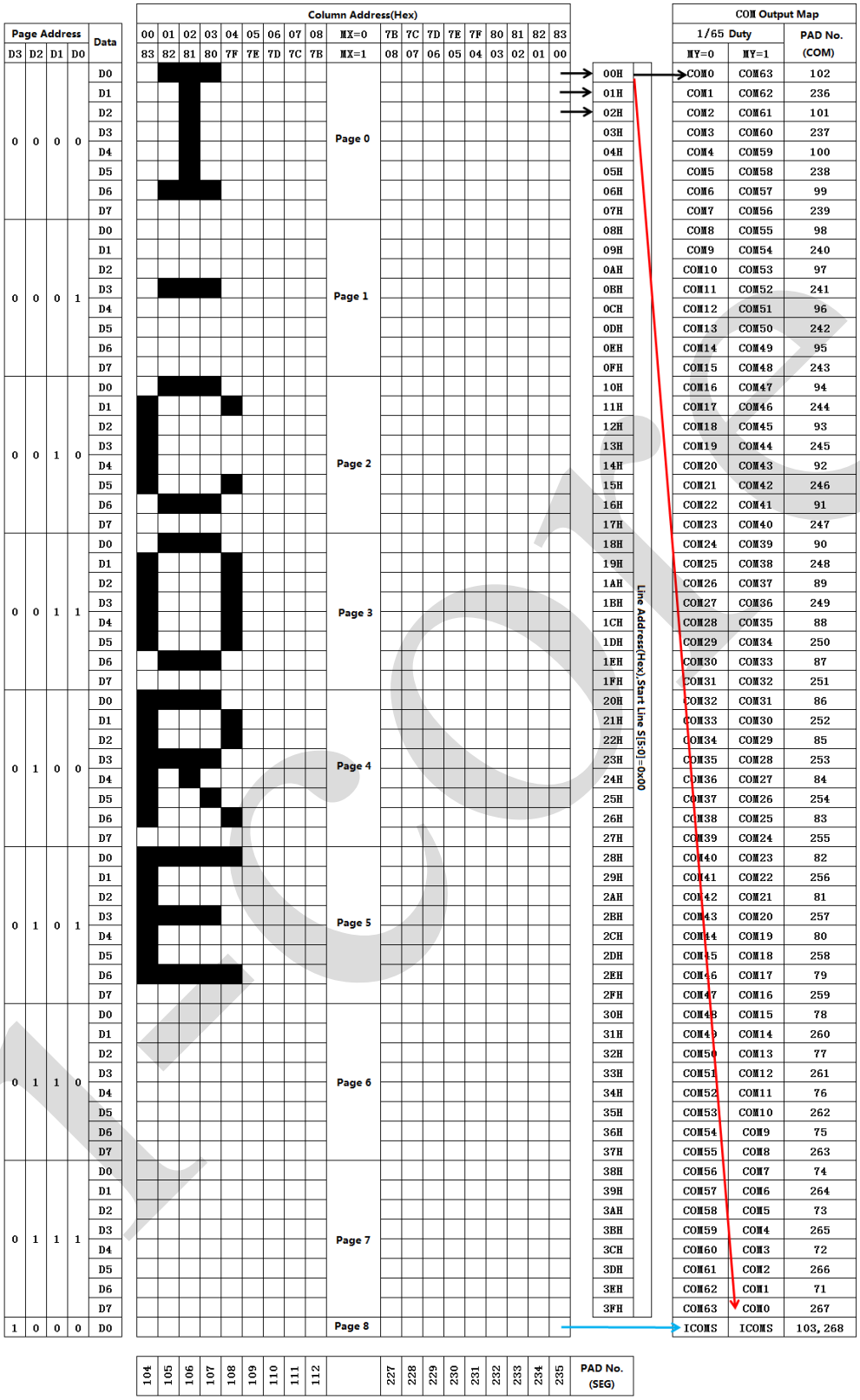


Figure 21. DDRAM and Output Map (COM/SEG) 1/65Duty

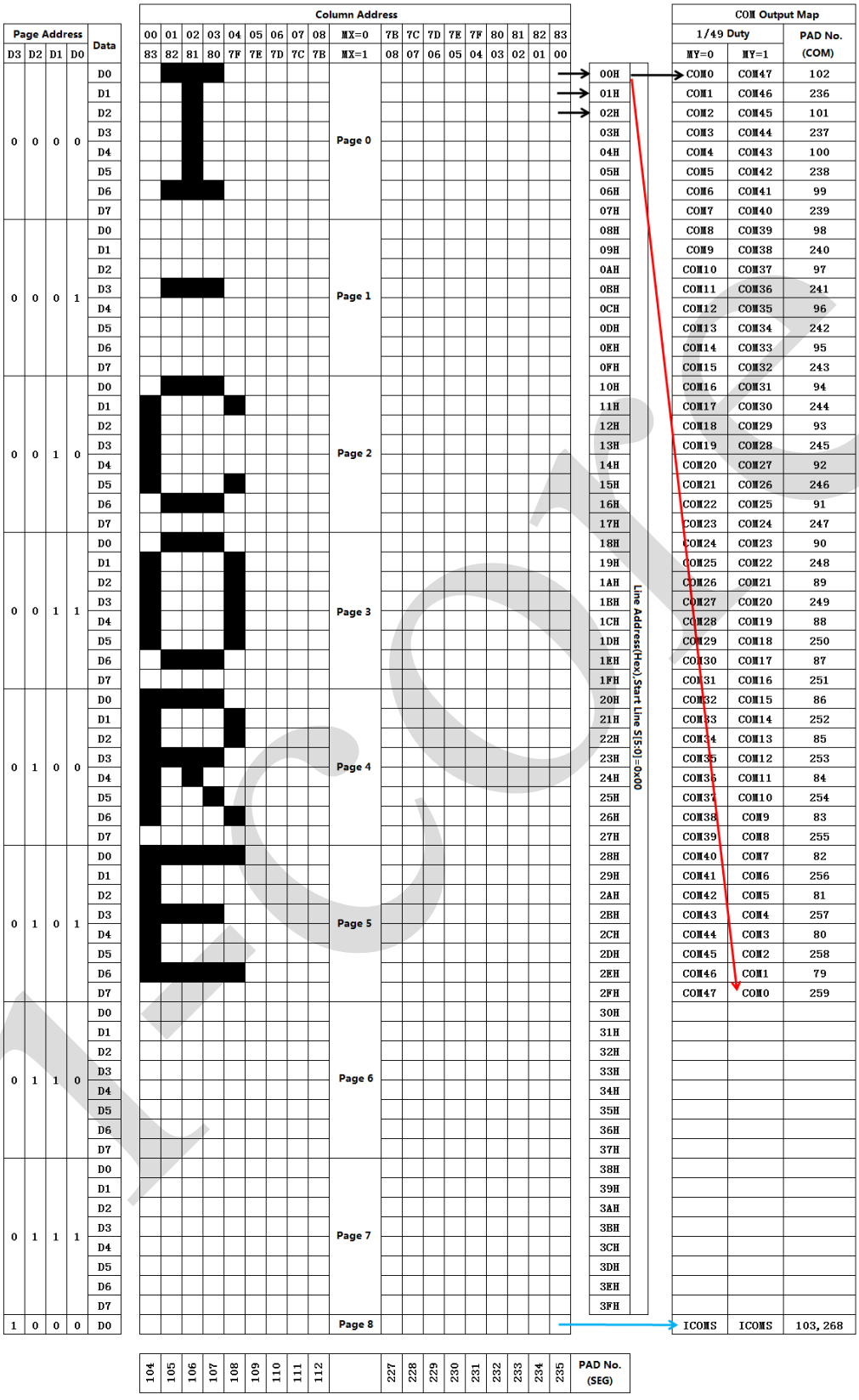


Figure 22. DDRAM and Output Map (COM/SEG) 1/49Duty

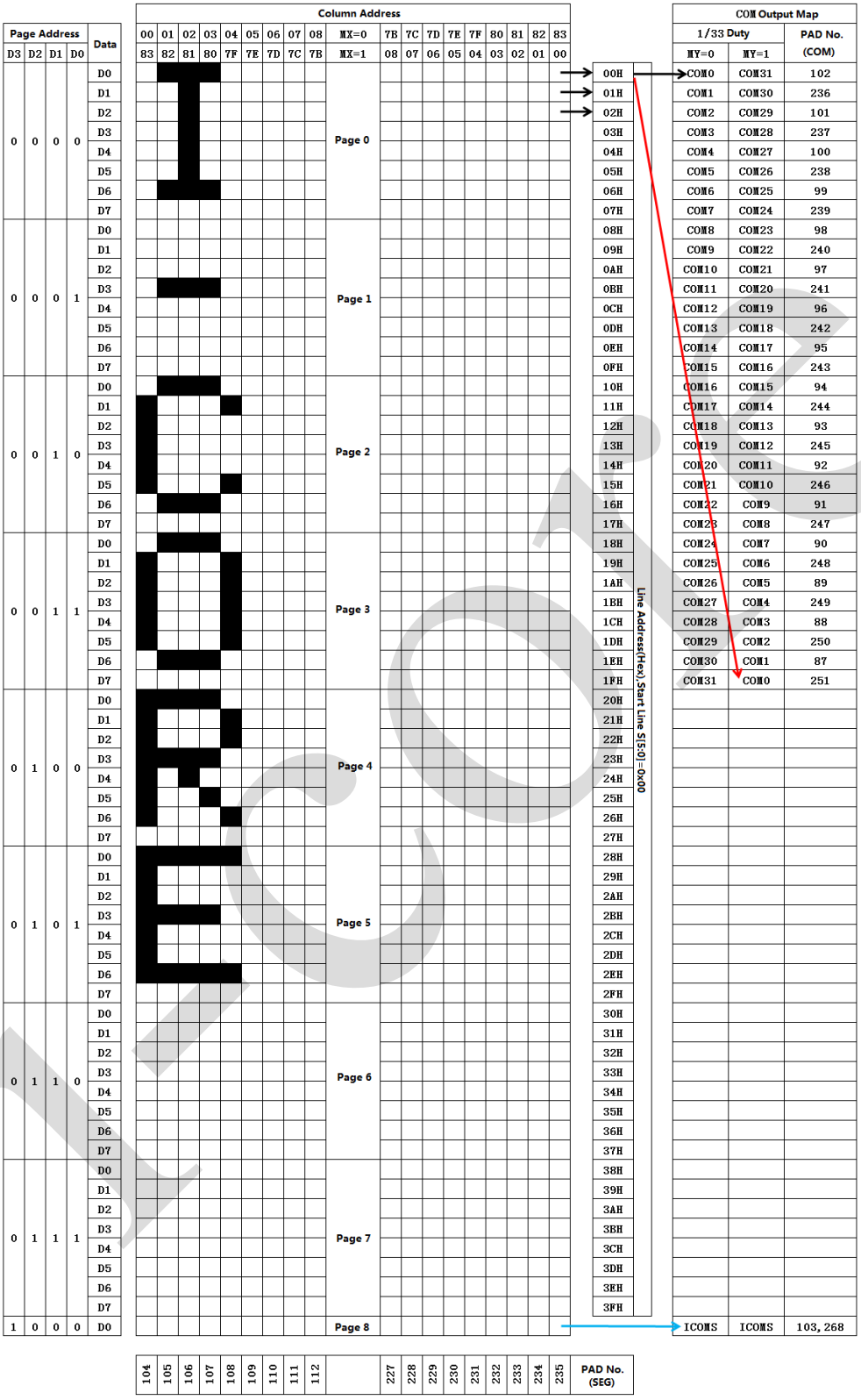


Figure 23. DDRAM and Output Map (COM/SEG) 1/33Duty

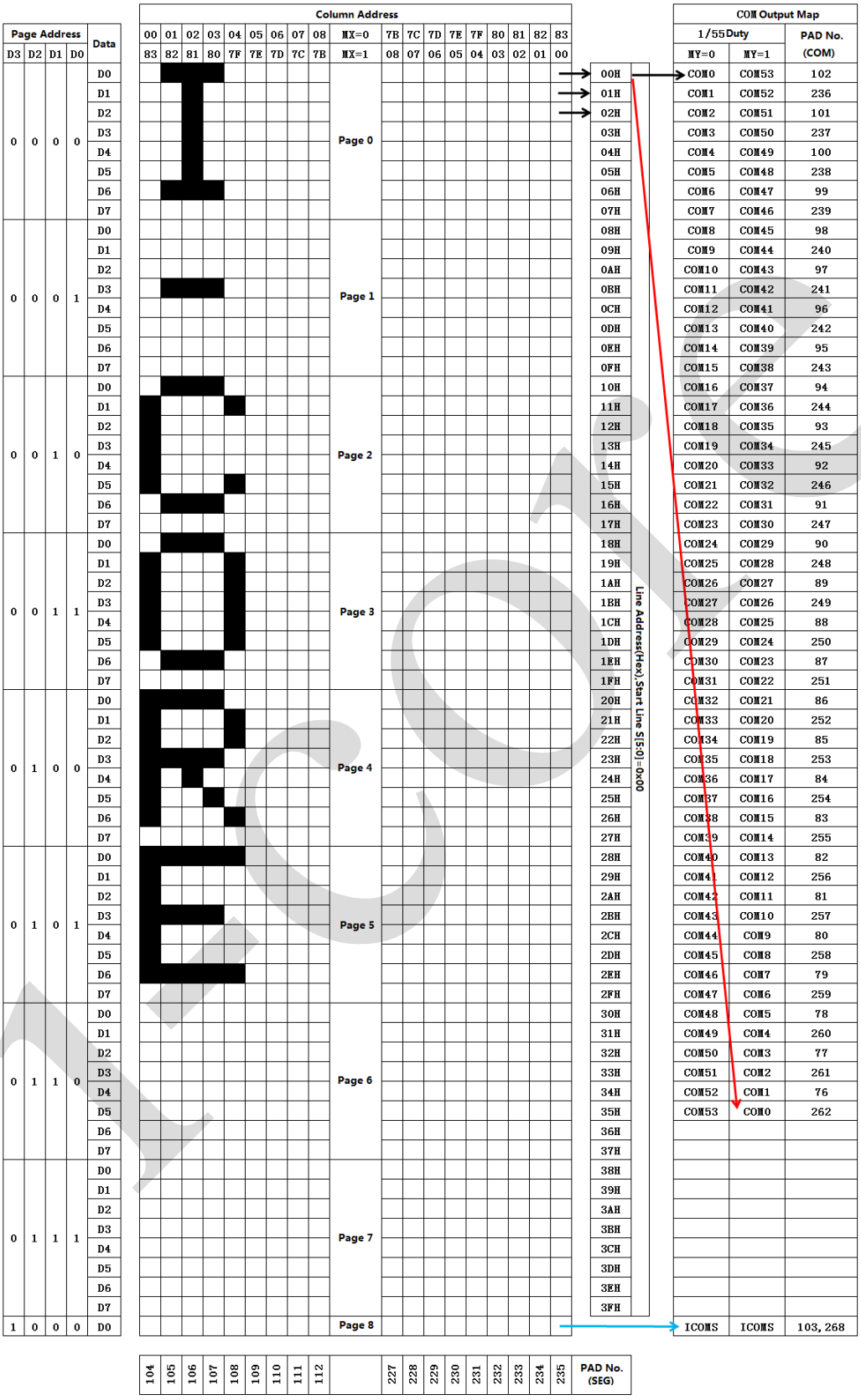


Figure 24. DDRAM and Output Map (COM/SEG) 1/55Duty

4.7.3、Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the “Display Start Line Set” instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore, by setting Line Address repeatedly, AiP31567A can realize the screen scrolling without changing the contents of DDRAM as shown in Figure 25. The last common is always the COMS (common output for the icons). That means the icons will never scroll with the general display data.

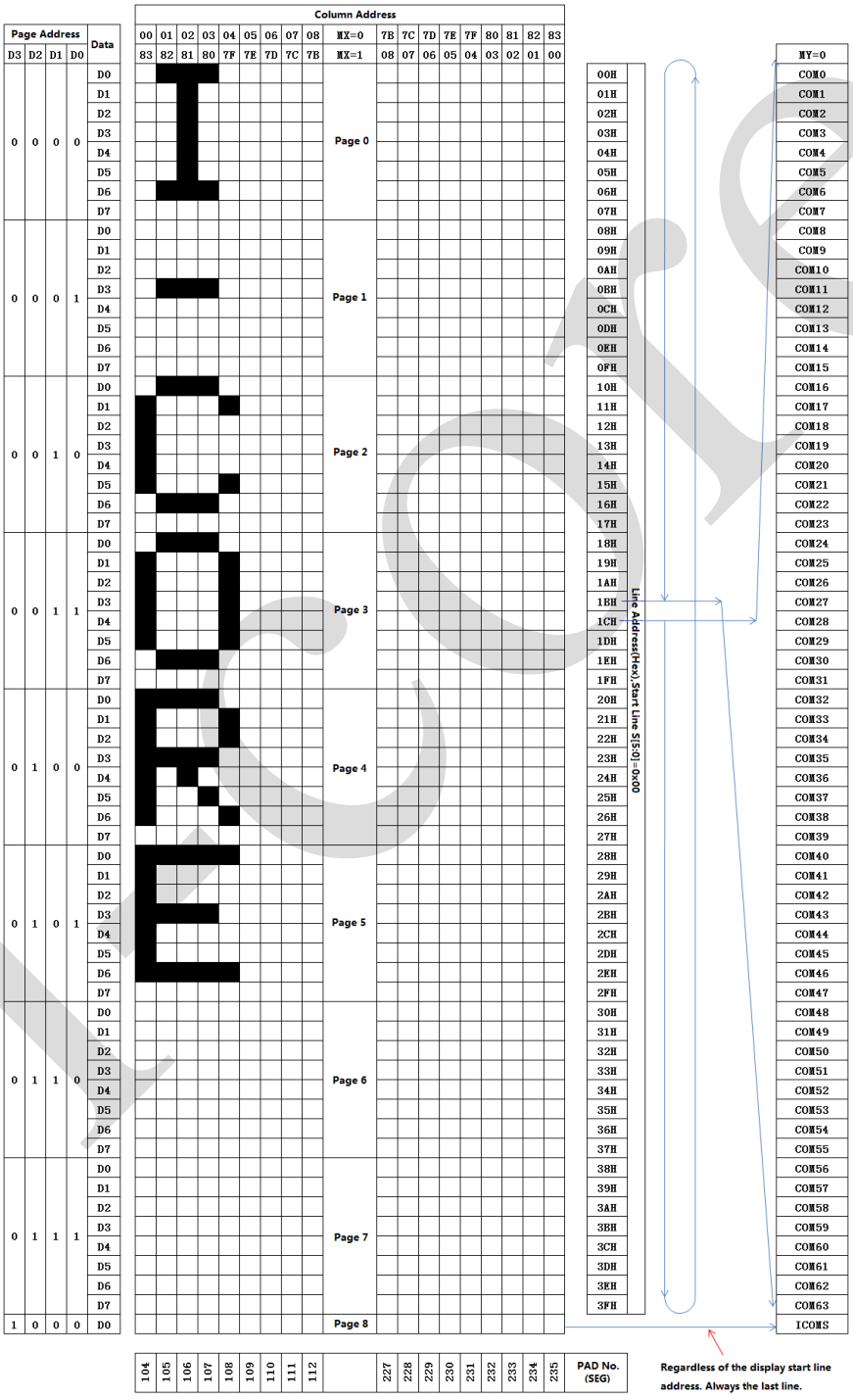


Figure 25. Start Line Function

4.8、Display Data Latch Circuit

The display data latch circuit latches temporarily display data of each segment output which will be output at the next clock. The special functions such as reverse display, display OFF and display all points ON only change the data in the latch and the content in the Display Data RAM is not changed.

4.9、Oscillation Circuit

The built-in oscillation circuit generates the system clock for the liquid crystal driving circuit. The oscillation circuit is enabled after initializing AiP31567A. The clock will not be output to reduce the power consumption.

4.10、Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external components. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power AiP31567A OFF, a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

4.11、External Components of Power Circuit

Recommended power circuit peripherals have only two capacitors. The value of these two capacitors are decided by the panel size or the loading.

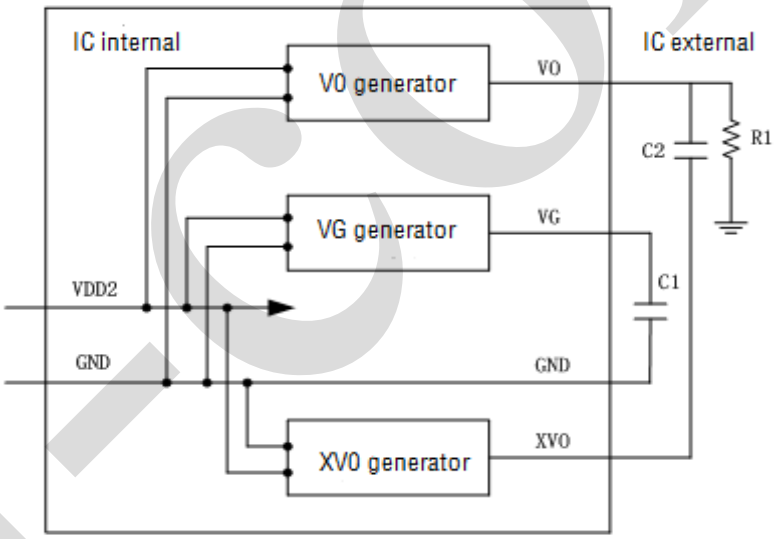


Figure 26. Power Circuit (C1, C2, R1 default N.C.)

Components selection notes:

[1] If the panel size is larger than 2” or heavy loading, the capacitor C1 and C2 must be added.

[2] If the icon is used, the capacitor C1 and C2 must be added.

[3] If the module is abnormal power down or do not follow the power off sequence, the resistor R1 can be added according to the display performance on LCD panel.

[4] The referential external component value:

C1=0.1uF~1.0uF (Non-Polar/25V, default N.C.)

C2=0.1uF~1.0uF (Non-Polar/6V, default N.C.)

R1=500KΩ~1MΩ (default N.C.)

Higher capacitor values are recommended for ripple reduction.

[5] In high power mode, C2 must be connected.

4.12、Regulator Circuit

The built-in high accuracy regulation circuit has 8 regulation ratios and each one has 64 EV-levels for voltage adjustment. Without additional external component, the output voltage can be changed by instructions such as “Regulation Ratio” and “Set EV”. The detailed setting method can be found in the INSTRUCTION DESCRIPTION section.

4.13、Reset Circuit

Setting RSTB to “L” can initialize internal function. While RSTB is “L”, no instruction except read status can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. Please note the hardware reset is not same as the software reset. When RSTB becomes “L”, the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

Procedure	Hardware Reset	Software Reset
Display OFF: D=0, all SEGs/COMs output at GND	V	X
Normal Display: INV=0, AP=0	V	X
SEG Normal Direction: MX=0	V	X
Clear Serial Counter and Shift Register (if using Serial Interface)	V	X
Bias Selection: BS=0	V	X
Booster Level BL=0	V	X
Exit Power Saving Mode	V	X
Power Control OFF: VB=0, VR=0, VF=0	V	X
N-Line Inversion NL[4:0] = (0, 1, 1, 0, 0)	V	X
Extension Command Set: Mode=0	V	X
Display Setting Mode: DSM=0	V	X
Duty: DT[3:0]=(0,0,0,0)	V	X
Set Bias: BA[2:0]=(0,0,0)	V	X
Frame Rate: FR[2:0]=(0,0,0)	V	X
Exit Read-modify-Write mode	V	V
Start Line S[5:0]=0	V	V
Column Address X[7:0]=0	V	V
Page Address Y[3:0]=0	V	V
COM Normal Direction: MY=0	V	V
V0 Regulation Ratio RR[2:0]=(1,0,0)	V	V
EV[5:0]=(1,0,0,0,0,0)	V	V

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

4.14、Instruction

4.14.1、Instruction Table

No.	Instruction	A0	R/W (RWR)	Command Byte								description
				D7	D6	D5	D4	D3	D2	D1	D0	
1	Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON; D=0, display OFF
2	Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
3	Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
4	Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
		0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
5	Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
6	Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
7	Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
8	SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
9	Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
10	All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
11	Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
12	Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0; Write:+1
13	END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
14	RESET	0	0	1	1	1	0	0	0	1	0	Software reset
15	COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
16	Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
17	Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
18	Set EV	0	0	1	0	0	0	0	0	0	1	Double command Set electronic volume (EV) level
		0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
19	Set Booster	0	0	1	1	1	1	1	0	0	0	Double command Set booster level: BL=0: 4X BL=1: 5X
		0	0	0	0	0	0	0	0	0	BL	
20	Power Save	0	0	(1) + (10) compound command								Display OFF & All Pixel ON

21	NOP	0	0	1	1	1	0	0	0	1	1	No operation
22	Set N-Line	0	0	1	0	0	0	0	1	0	1	Set N-Line inversion
		0	0	0	0	0	NL4	NL3	NL2	NL1	NL0	
23	Release N-Line	0	0	1	0	0	0	0	1	0	0	Exit N-Line inversion
24	SPI Read Status	0	1	1	1	1	1	1	1	0	0	SPI read status command
		0	1	0	MX	D	RST	ID3	ID2	ID1	ID0	SPI read DDRAM command
25	SPI Read DDRAM	0	1	1	1	1	1	1	1	0	1	SPI read DDRAM command
		1	1	D7	D6	D5	D4	D3	D2	D1	D0	SPI read DDRAM
Extension Command Set												
-	Extension Command Set	0	0	1	1	1	1	1	1	1	mode	Mode=1: Enter extension command table Mode=0: Exit extension command table
1	High Power Mode ON	0	0	0	1	1	0	1	0	1	1	Enter high power mode
2	High Power Mode OFF	0	0	0	1	1	0	0	1	0	0	Exit high power mode
3	Display Setting Mode	0	0	0	1	1	1	-	-	DSM	0	Complex command DSM=1: Enter display setting DSM=0: Exit display setting When DSM=1, Set duty(DT[3:0]), bias(BA[2:0]), frame rate(FR[2:0])
		0	0	1	1	0	1	DT3	DT2	DT1	DT0	
		0	0	1	0	0	1	0	BA2	BA1	BA0	
		0	0	1	0	0	1	1	FR2	FR1	FR0	

Notes:

[1] Symbol "-" means this bit can be "H" or "L".

[2] Do not use instructions not listed in these tables.

4.14.2、Display ON/OFF

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	D

D=1: Normal Display Mode.

D=0: Display OFF. All SEGs/COMs output with GND.

4.14.3、Set Start Line

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S5	S4	S3	S2	S1	S0

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
…	…	…	…	…	…	…
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

4.14.4、Set Page Address

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	Y3	Y2	Y1	Y0

Y [3:0] defines the Y address vector address of the display RAM.

Y3	Y2	Y1	Y0	Page Address	Valid Bit
0	0	0	0	Page 0	D0~D7
0	0	0	1	Page 1	D0~D7
0	0	1	0	Page 2	D0~D7
…	…	…	…	…	…
0	1	1	0	Page 6	D0~D7
0	1	1	1	Page 7	D0~D7
1	0	0	0	Page 8 (icon page)	D0

4.14.5、Set Column Address

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	X7	X6	X5	X4
0	0	0	0	0	0	X3	X2	X1	X0

The range of column address is 0…131. The parameter is separated into 2 instructions.

X7	X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2

0	0	0	0	0	0	1	1	3
…	…	…	…	…	…	…	…	…
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

4.14.6、Read Status

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	MX	D	RST	0	0	0	0

Read the internal status of AiP31567A.

MX=0: Normal direction (SEG0->SEG131);

MX=1: Reverse direction (SEG131->SEG0).

D=0: Display ON;

D=1: Display OFF.

RST=1: During reset (hardware or software reset)

RST=0: Normal operation

4.14.7、Write Data

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

4.14.8、Read Data

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read data							

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

4.14.9、SEG Direction

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

MX=0: Normal direction (SEG0->SEG131);

MX=1: Reverse direction (SEG131->SEG0).

4.14.10、Inverse Display

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

INV=0: Normal display;

INV=1: Inverse display.

4.14.11、All Pixel ON

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

AP=0: Normal display;

AP=1: All pixels ON.

4.14.12、Bias Select

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	BS

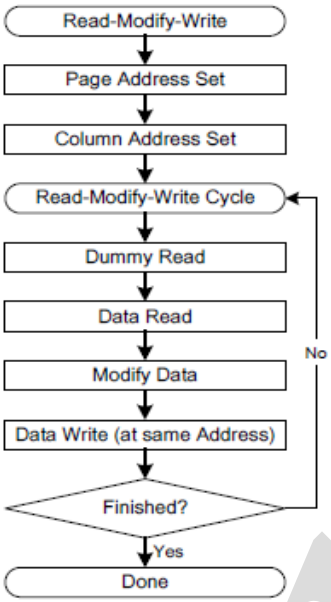
Duty	Bias	
	BS=0	BS=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

Symbol	Bias voltage
V0	V0
VG	2/9×V0
VM	1/9×V0
GND	GND

4.14.13、Read-modify-Write

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	0

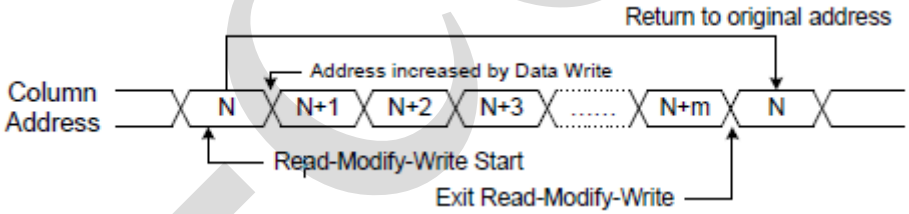
This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.



4.14.14、END

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.



4.14.15、RESET

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

Please note this instruction is not complete same as hardware reset (RSTB=L) and cannot initialize the built-in power circuit which is initialized by the RSTB pin.

4.14.16、COM Direction

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	MY	-	-	-

MY=0: Normal direction (COM0->COM63);

MY=1: Reverse direction (COM63->COM0).

4.14.17、Power Control

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	VB	VR	VF

VB=0: Built-in Booster OFF;

VB=1: Built-in Booster ON.

VR=0: Built-in Regulator OFF;

VR=1: Built-in Regulator ON.

VF=0: Built-in Follower OFF;

VF=1: Built-in Follower ON.

4.14.18、Regulation Ratio

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	RR2	RR1	RR0

RR2	RR1	RR0	Regulation Ratio (RR)
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

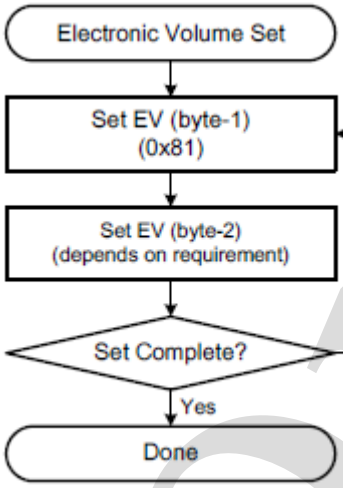
The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0]) V0=RR×[1–(63–EV)/162] ×2.1, or V0=RR×[(99+EV)/162] ×2.1.

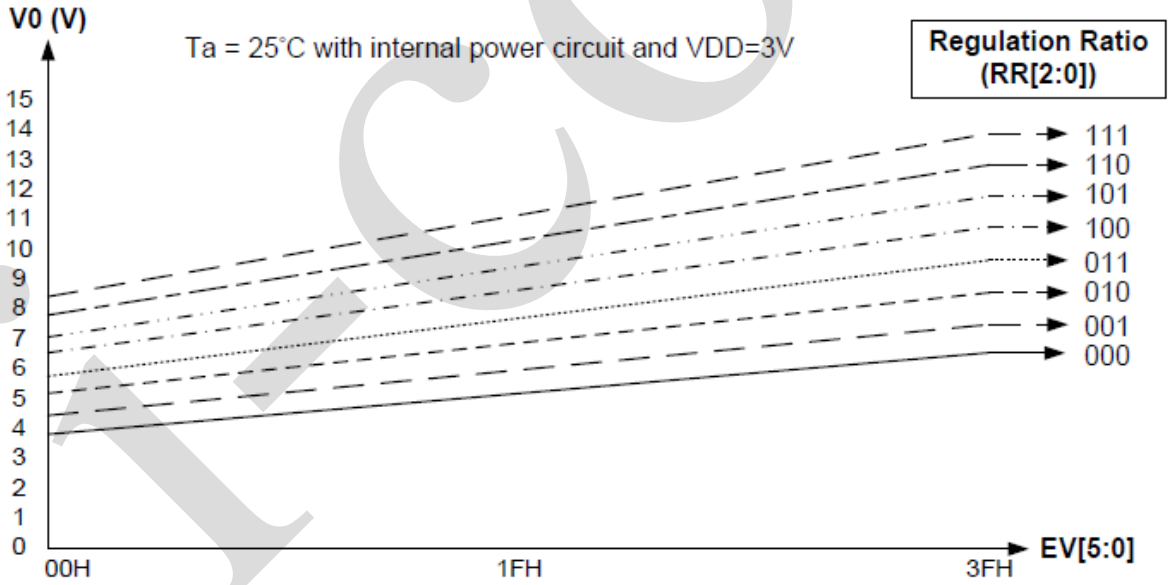
Symbol	Register	Value
RR	RR[2:0]	3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5
EV	EV[5:0]	0~63

4.14.19、Set EV

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0

That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.





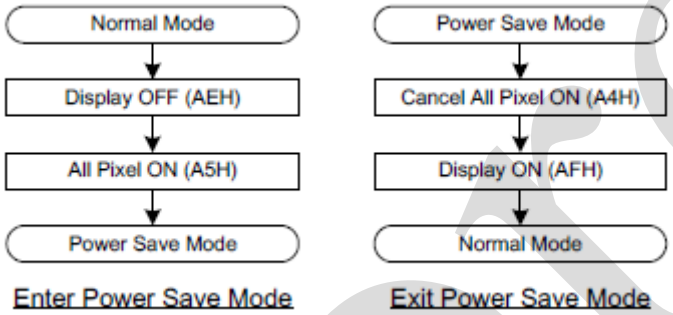
EV[5:0] and RR[2:0] vs. V0 Voltage

4.14.20、Power Save

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	0
0	0	1	0	1	0	0	1	0	1

This is compound instruction. The 1st instruction is Display OFF (D=0) and the 2nd instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure:

1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at GND.



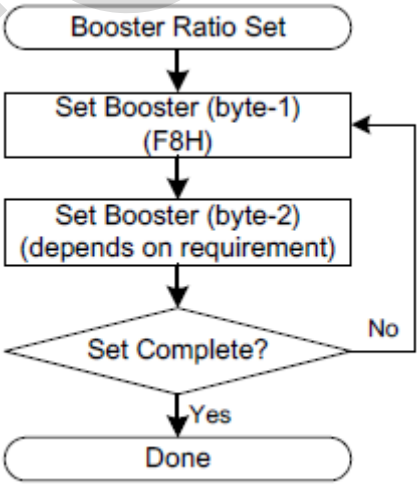
After exiting Power Save mode, the settings will return to be as they were before.

4.14.21、Set Booster

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	0	0	0
0	0	0	0	0	0	0	0	0	BL

BL=0: Boost level=X4;

BL=1: Boost level=X5.



4.14.22、NOP

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

AiP31567A will do nothing when receiving this instruction.

4.14.23、Set N-Line

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	1	0	1
0	0	0	0	0	NL4	NL3	NL2	NL1	NL0

This 2-byte instruction sets the inverted line number within range of 1 to 32 to improve the display quality by controlling the phase of the internal frame signal. The DC bias maybe occurred if the N-line is not set well. Be sure to confirm this factor after choosing a value of N.

NL4	NL3	NL2	NL1	NL0	Selected N-Line Inversion
0	0	0	0	0	1-line inversion
0	0	0	0	1	2-line inversion
0	0	0	1	0	3-line inversion
0	0	0	1	1	4-line inversion
…	…	…	…	…	…
1	1	1	1	0	31-line inversion
1	1	1	1	1	32-line inversion

4.14.24、Release N-Line

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	1	0	0

This instruction makes the inversion mode back to the frame inversion from the N-Line inversion.

4.14.25、SPI Read Status

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1	1	0	0
0	1	0	MX	D	RST	ID3	ID2	ID1	ID0

4.14.26、SPI Read DDRAM

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1	1	0	1
1	1	D7	D6	D5	D4	D3	D2	D1	D0

4.14.27、Extension Command Set

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	0	Mode

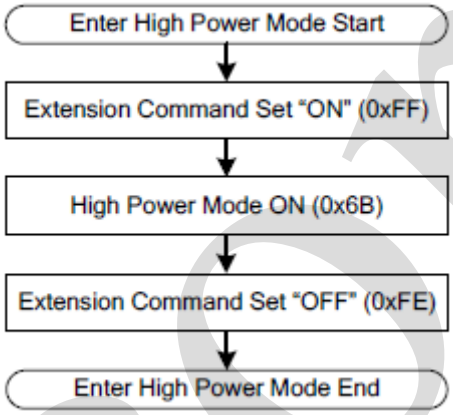
Mode=0: Exit extension command set;

Mode=1: Enter extension command set.

4.14.28、High Power Mode

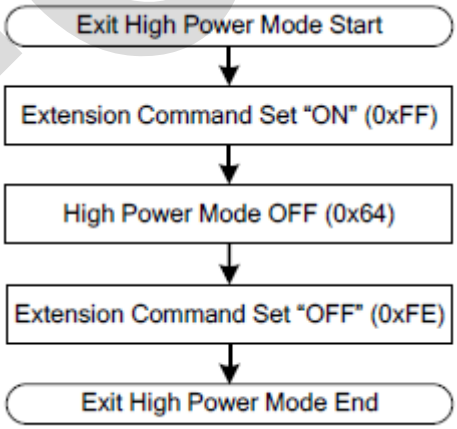
A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	1	0	1	1

This instruction makes the High Power Mode turn on. This feature should be turned on when the VG exceed VDD.



A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1	0	0

This instruction makes the High Power Mode turn off.



4.14.29、Display Setting Mode

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	-	-	DSM	0
0	0	1	1	0	1	DT3	DT2	DT1	DT0
0	0	1	0	0	1	0	BA2	BA1	BA0
0	0	1	0	0	1	1	FR2	FR1	FR0

DSM=0: Exit display setting mode;

DSM=1: Enter display setting mode.

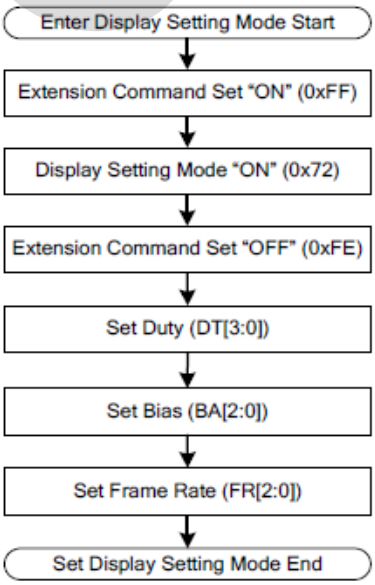
This instruction enables Display Setting Mode. The duty, bias, and frame rate must be initialized by command when display setting mode is enabled.

DT[3:0] sets the display duty and has priority over the SEL[2:1].

DT3	DT2	DT1	DT0	Selected Duty Ratio
0	1	0	0	65 (1/64+1 icon)
0	1	1	1	55 (1/54+1 icon)
0	1	0	1	49 (1/48+1 icon)
0	1	1	0	33 (1/32+1 icon)
1	1	1	0	17 (1/16+1 icon)
1	0	1	0	9 (1/8+1 icon)

FR[2:0] specifies the frame rate for different duty.

FR2	FR1	FR0	Frame Rate(Hz)	
			9 duty ~ 17 duty	33 duty ~ 65 duty
0	0	0	70	75
0	0	1	105	110
0	1	0	140	150
0	1	1	175	190
1	0	0	195	220
1	0	1	230	250
1	1	0	275	300



4.15、Operation Flow

4.15.1、Power ON

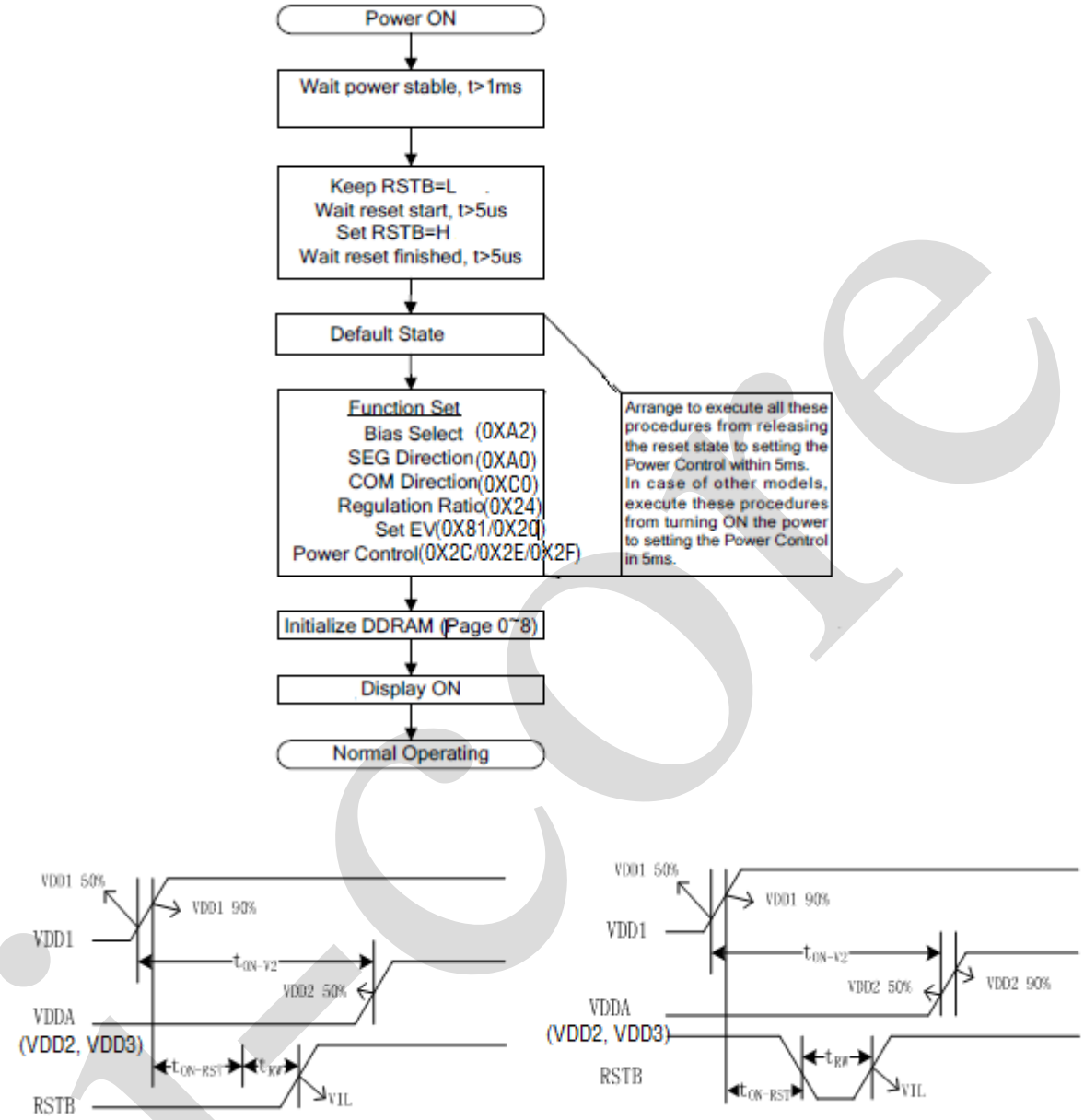


Figure 24. RSTB=L or H, while Power ON

Note: The detailed description can be found in the respective sections listed below.

[1] Please refer to the timing specification of t_{RW} and t_R.

[2] More details about RESET refer to 4.13

[3] The 5ms requirement depends on the characteristics of LCD panel and the external component of the power circuit. It is recommended to check with the real products with external component.

[4] The detailed instruction functionality is described in 4.14.

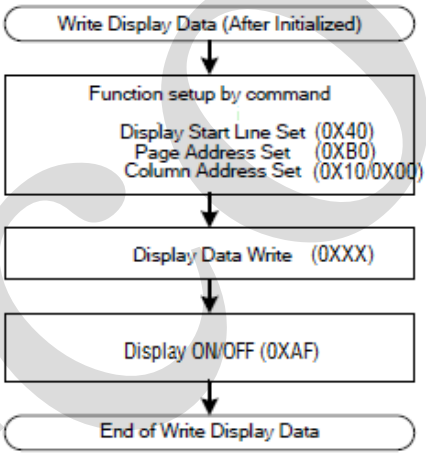
[5] Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

4.15.2、Timing Requirement

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	Applying VDDI and VDDA in any order will not damage IC.
RSTB input time	t_{ON-RST}	no limitation	1. If RSTB is Low, High or unstable during power ON, a successful hardware reset by RSTB is required after VDDI is stable. 2. RSTB=L can be input at any time after power is stable. 3. t_{RW} and t_R should match the timing specification of RSTB. 4. To prevent abnormal display, the recommended timing is: 1ms≤t_{ON-RST} ≤30ms.

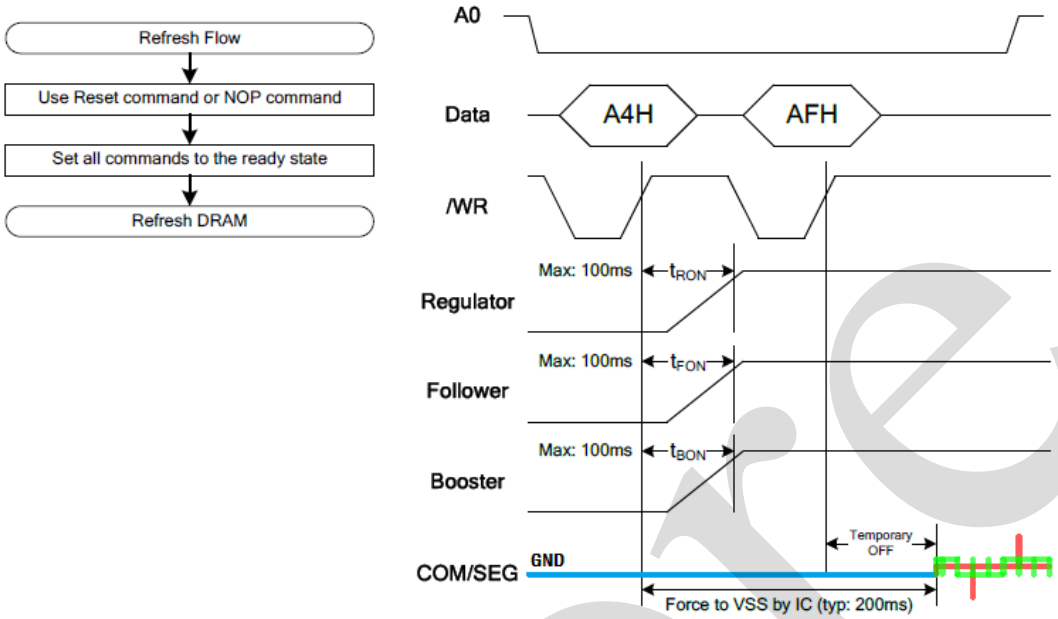
Note: The requirement listed here is to prevent abnormal display on LCD module.

4.15.3、Display Data



4.15.4、Refresh

It is recommended to use the refresh sequence regularly in a specified interval.



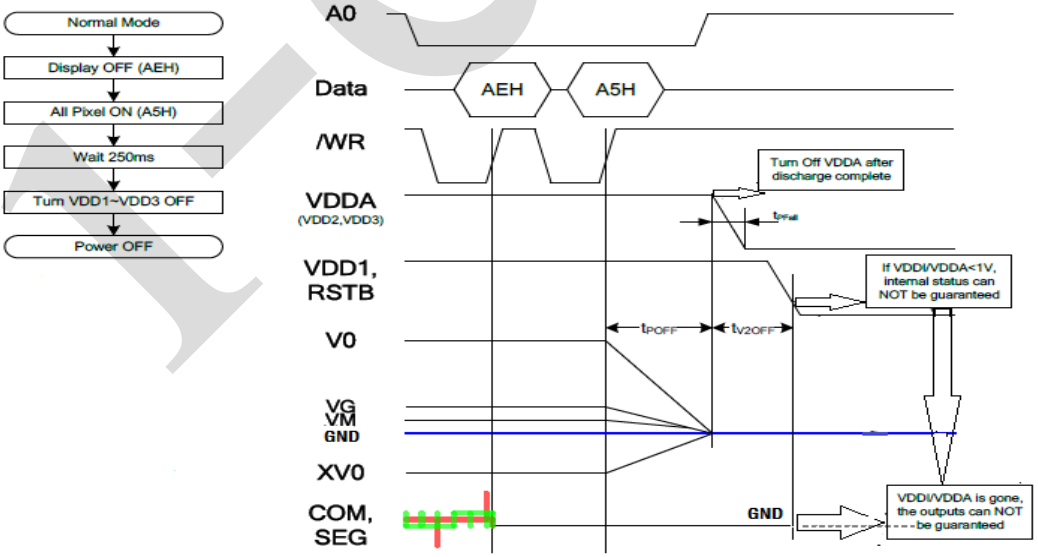
Note:

[1] The power stable time is determined by LCD panel loading.

[2] The power stable time in this figure is base on: LCD Panel Size=1.4 without capacitor (VDD=2.7V, Vop=9V).

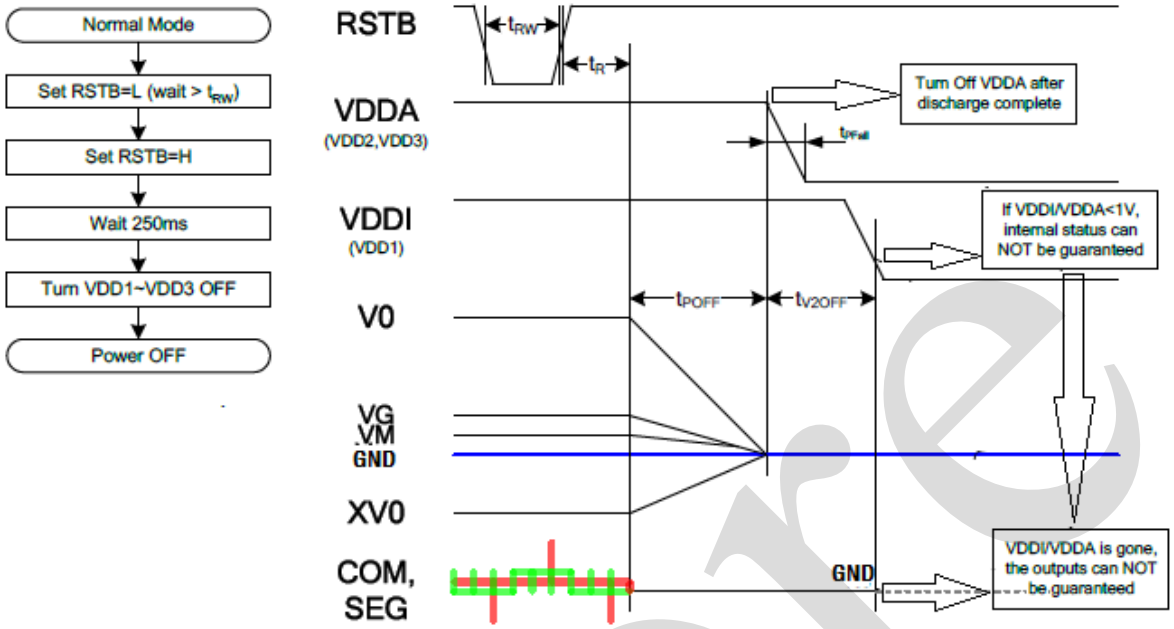
4.15.5、Power OFF Flow and Sequence (use power save instruction)

In power save mode, LCD outputs are fixed to GND and all analog outputs are discharged. The power can be turned OFF after AiP31567A is in the power save mode.



After the built-in power circuits are OFF and completely discharged, the power (VDDI, VDDA) can be removed.

4.15.6、Power OFF Flow and Sequence (use hardware reset function)



After the built-in power circuits are OFF and completely discharged, the power (VDDI, VDDA) can be removed.

Note:

[1] t_{POFF}: Internal Power discharge time. -->250ms (max).

[2] t_{V2OFF}: Period between VDDI and VDDA OFF time.-->0ms (min).

[3] It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.

[4] IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.

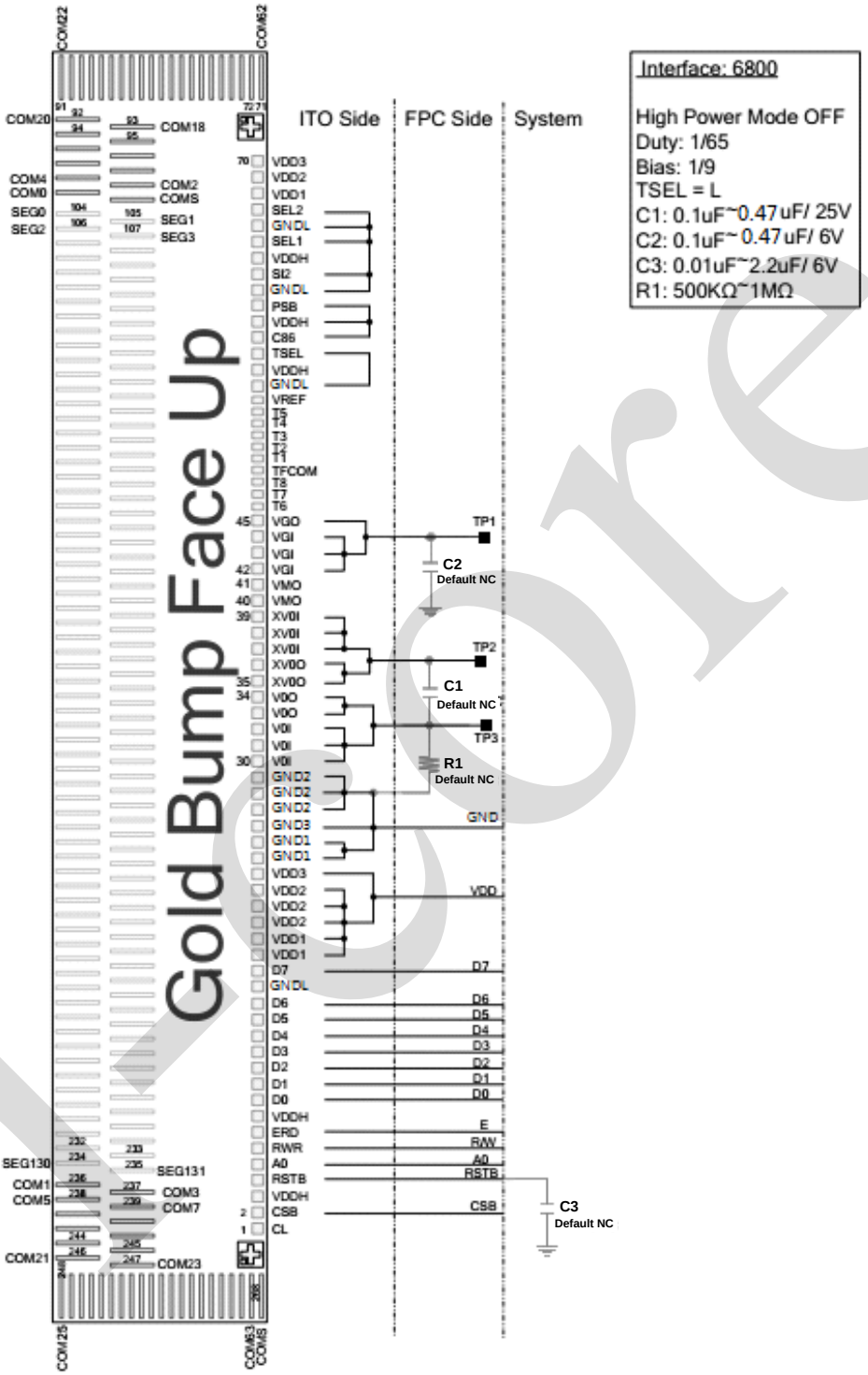
[5] The timing is dependent on panel loading and the external capacitor(s).

[6] The timing in these figures is base on the condition that: LCD Panel Size=1.4 without capacitor.

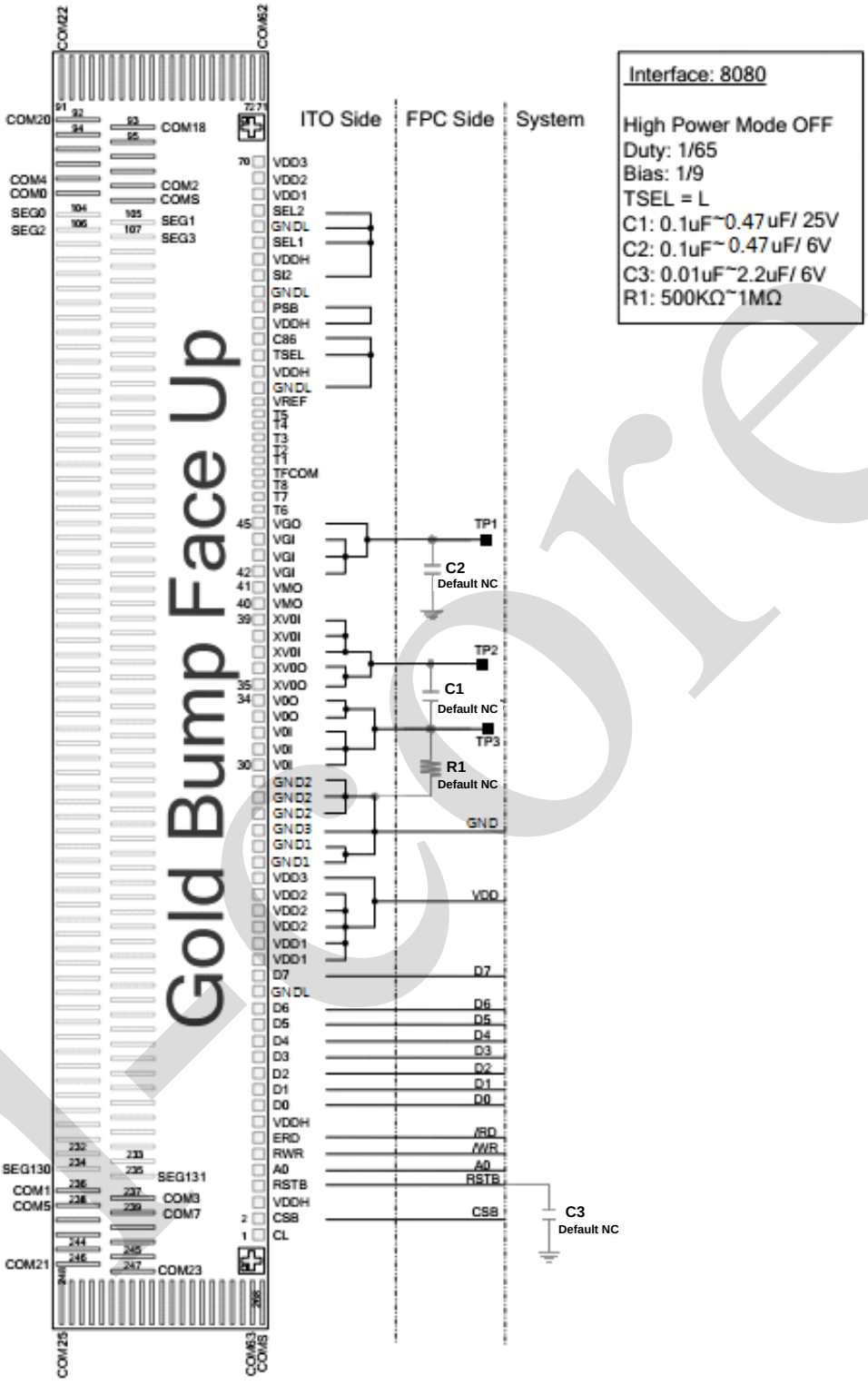
[7] When turning VDDA OFF, the falling time should follow the specification: 20ms≤ t_{Pfall} ≤0.2sec

5、Typical Application Circuit And Application Specification

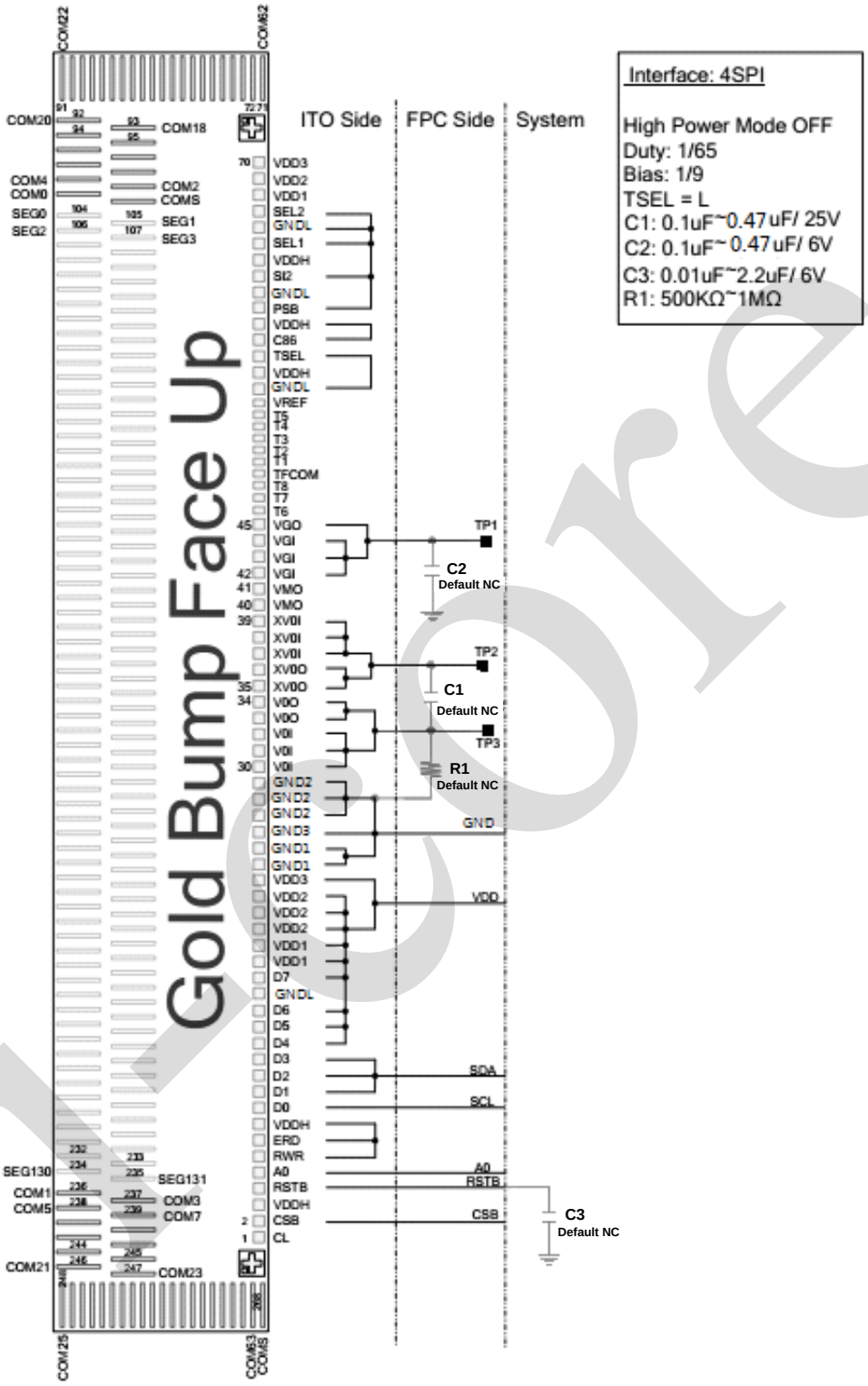
5.1、Application Circuit -- 6800 Interface



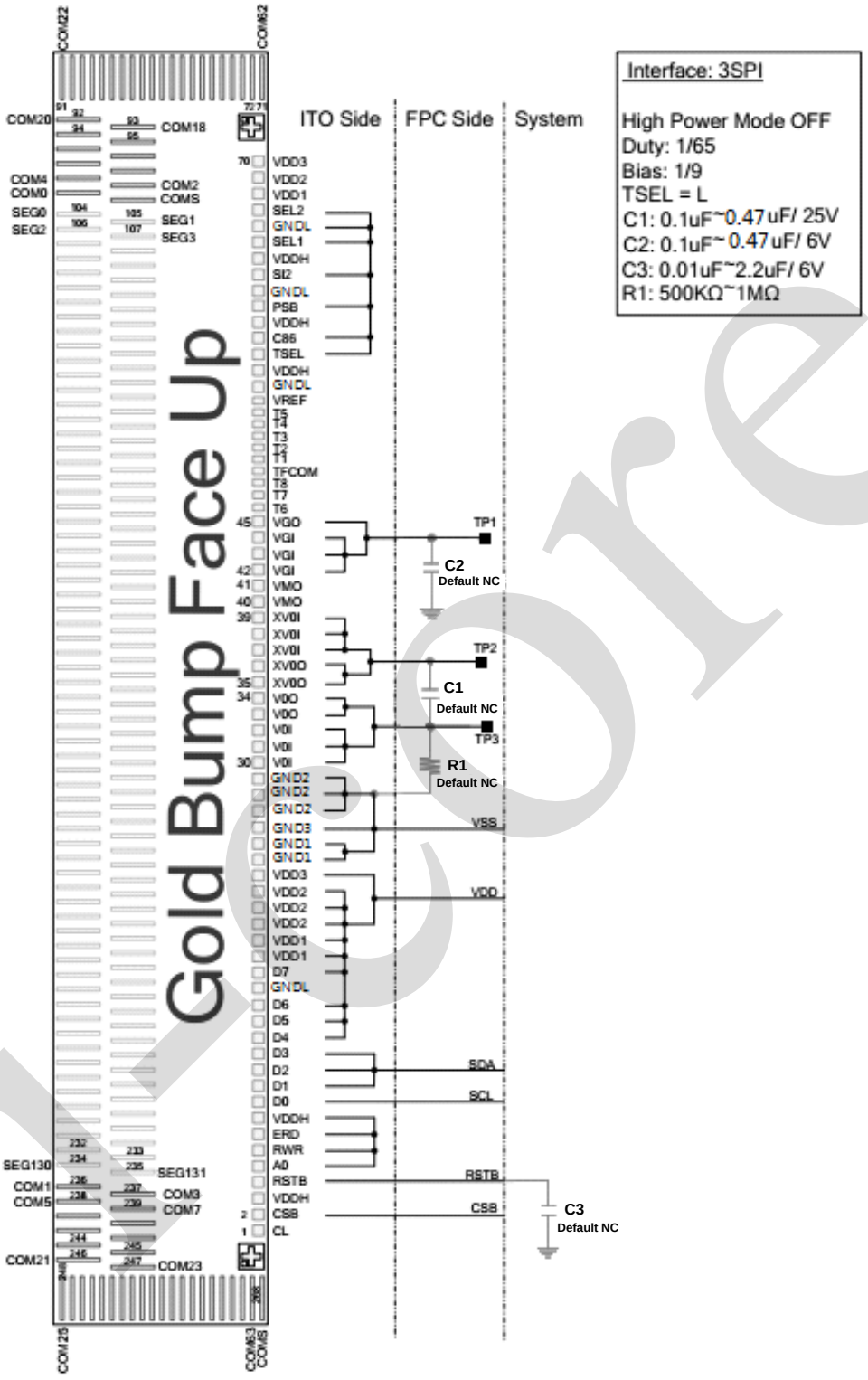
5.2、Application Circuit -- 8080 Interface



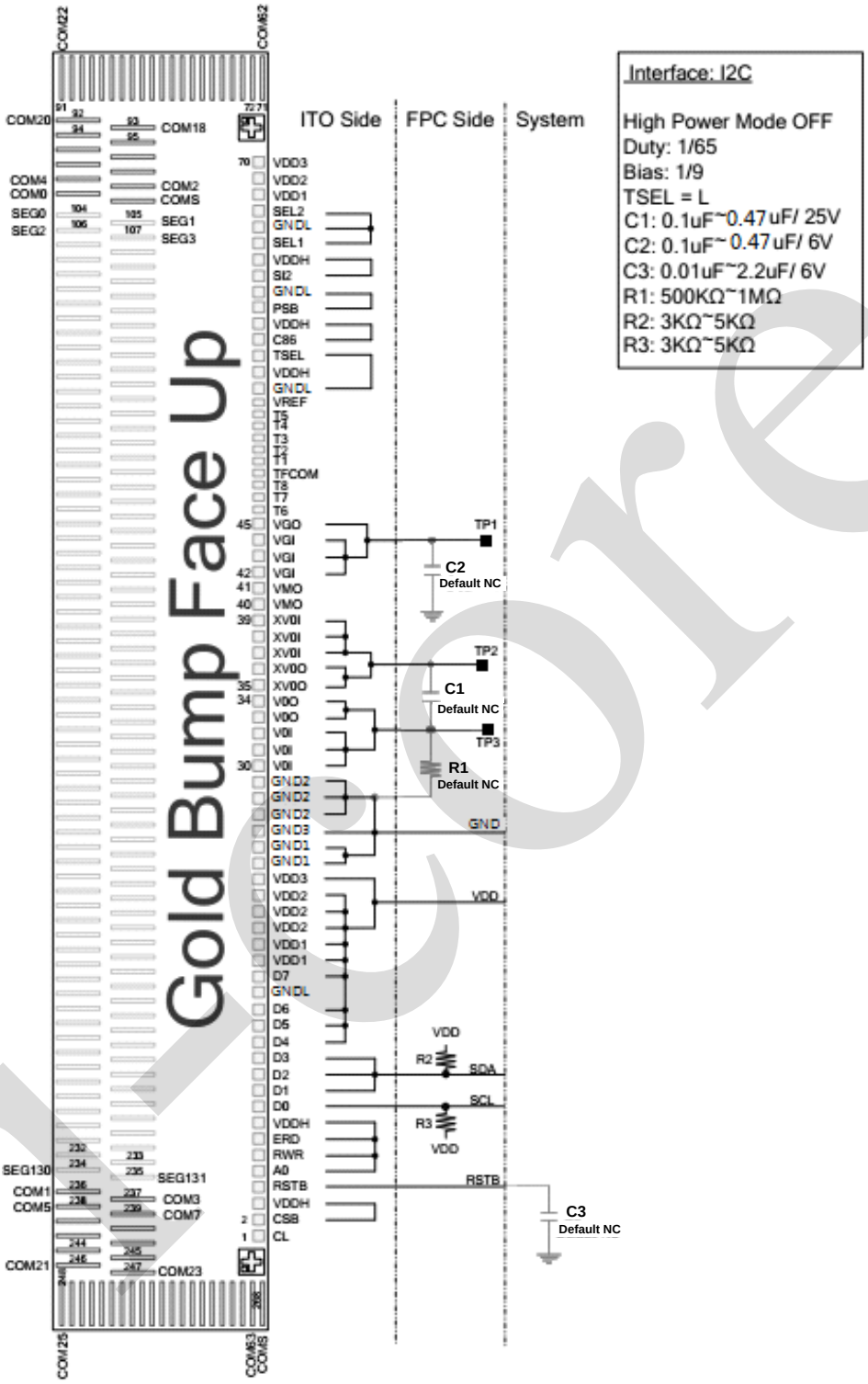
5.3、Application Circuit – 4-Line-SPI Interface



5.4、Application Circuit – 3-Line-SPI Interface



5.5、Application Circuit –I2C Interface



5.6、Application Specification

5.6.1、Selection of Application Voltage

[1] Positive Booster: (VDD2×BL×BE) ≥ V0 or (VDD2×BL×BE) ≥ Vop.

[2] Negative Booster: [–VDD2×(BL – 1) ×BE] ≤ XV0 or [VDD2×(BL – 1) ×BE] ≥ (Vop–VG), where VG=Vop×2/N.

[3] If VG≥VDD2-0.2V, please enable high power mode.

[4] Vop requirement: [VDD2×(BL – 1) ×BE] ≥ [Vop×(N–2)/N] or [Vop ≤ VDD2×(BL–1) ×BE×N/(N–2)].

[5] BL is the booster stage and BE is the booster efficiency. Referential values are listed below: (assume VDD2=VDD3=3.3V)

Module Size≤1.0: BE=90% (Typical);

Actual BE should be determined by module loading and ITO resistance value.

[6] The worse condition should be considered. Furthermore, it should reserve some range for the temperature compensation and the contrast control (for end-customer).

For quickly reference, the following table lists the EV setting range for Vop.

(VDD1=2.8V, VDD2=VDD3=2.8V, bare dice, T_{amb}=25℃)

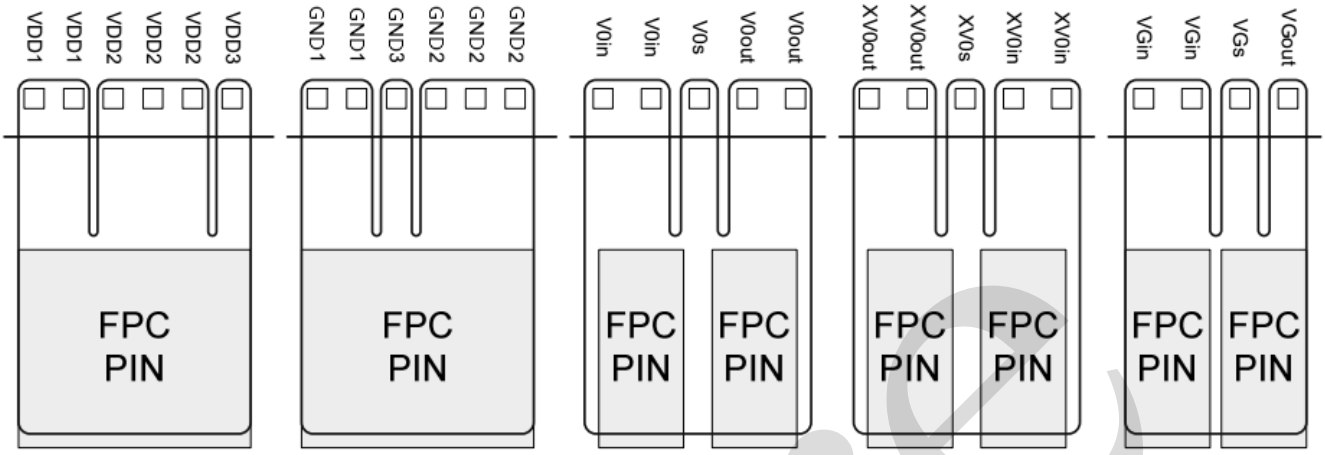
Bias	Booster	Vop	
		High Power Mode OFF	High Power Mode ON
1/9	X5	8.5~11.5	8.5~13.5
1/8	X5	7.5~10.0	7.5~13.5
1/7	X5	6.5~9.0	6.5~13.0
1/6	X5	5.5~7.5	5.5~11.0
1/5	X5	4.5~6.5	4.5~9.0
1/4	X5	4.0~5.0	4.0~7.0

(VDD1=2.8V, VDD2=VDD3=2.8V, bare dice, T_{amb}=25℃)

Bias	Booster	Vop	
		High Power Mode OFF	High Power Mode ON
1/9	X5	8.5~13.5	8.5~13.5
1/8	X5	7.5~12.0	7.5~13.5
1/7	X5	6.5~10.5	6.5~13.0
1/6	X5	5.5~9.0	5.5~11.0
1/5	X5	4.5~7.5	4.5~9.0
1/4	X5	4.0~6.0	4.0~7.0

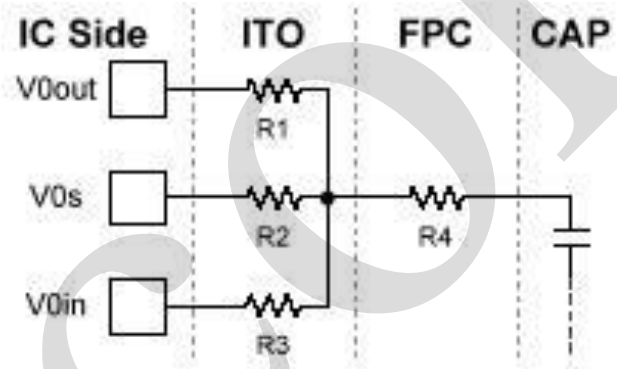
5.6.2、ITO Layout Reference

The reference ITO layout is shown below:



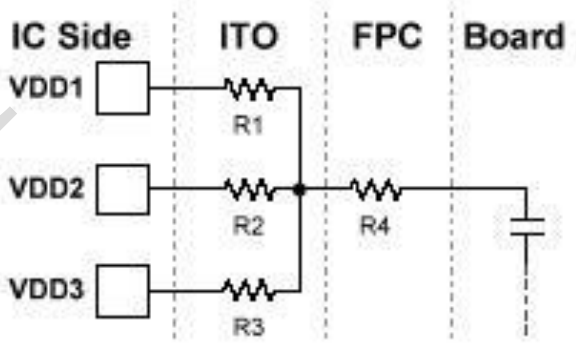
The equivalent circuit is shown below:

1. V0, XV0, VG



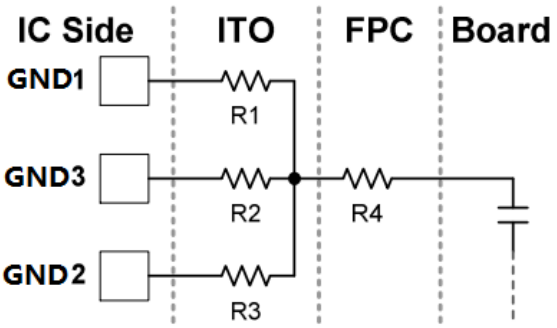
Ideal Layout: R4=0Ω, R2>>R1>R3
Acceptable Layout: R4≠0Ω, R2>>R1>R3>R4
Not Acceptable: R4≥ (R1 or R2 or R3)

2. VDD



Ideal Layout: R4=0Ω, R3>>R1>R2
Acceptable Layout: R4≠0Ω, R3>>R1>R2>R4
Not Acceptable: R4≥ (R1 or R2 or R3)

3. GND



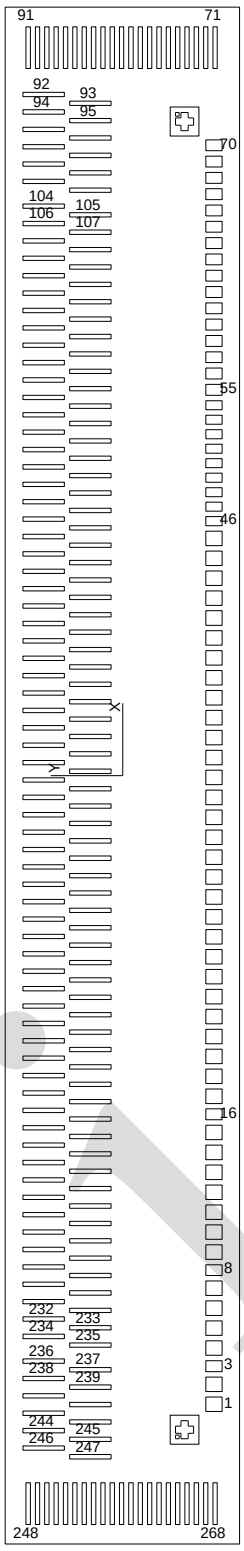
Ideal Layout: R4=0Ω, R2>>R1>R3

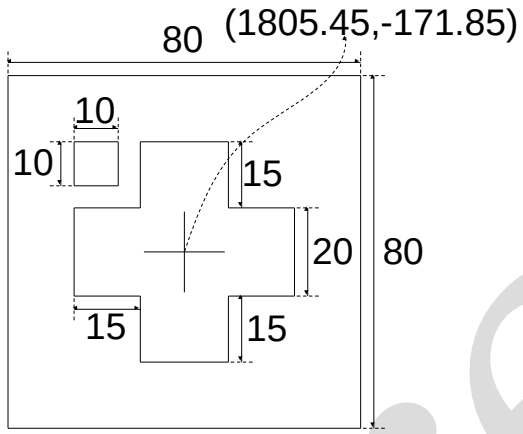
Acceptable Layout: R4≠0Ω, R2>>R1>R3>R4

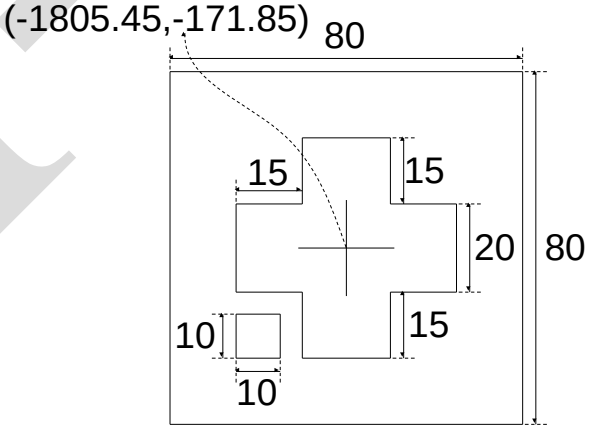
Not Acceptable: R4≥ (R1 or R2 or R3)

6、PAD And PAD Center Coordinates

6.1、PAD Arrangement







Chip Size	4242×652
Chip Thickness	300
Bump Height	9
Bump Size	
PAD No.	**Size**
71~91, 248~268	115×12
92~103, 104~235, 236~247	12×115
3, 8, 16, 55~70	30×45
46~54	25×45
1, 2, 4~7, 9~15, 17~45	40×45
Bump Space	
PAD No.	**Length**
1~70	15
71~91, 248~268	14
92~103, 104~235, 236~247	36
[1] Unit: um. [2] Refer to section "PAD CENTER COORDINATES" for ITO layout.	

6.2、PAD Center Coordinates

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	CL	-1735	-254.5	135	SEG31	828	89.5
2	CSB	-1680	-254.5	136	SEG32	804	219.5
3	VDDH	-1630	-254.5	137	SEG33	780	89.5
4	RSTB	-1580	-254.5	138	SEG34	756	219.5
5	A0	-1525	-254.5	139	SEG35	732	89.5
6	RWR	-1470	-254.5	140	SEG36	708	219.5
7	ERD	-1415	-254.5	141	SEG37	684	89.5
8	VDDH	-1365	-254.5	142	SEG38	660	219.5
9	D0	-1315	-254.5	143	SEG39	636	89.5
10	D1	-1260	-254.5	144	SEG40	612	219.5
11	D2	-1205	-254.5	145	SEG41	588	89.5
12	D3	-1150	-254.5	146	SEG42	564	219.5
13	D4	-1095	-254.5	147	SEG43	540	89.5
14	D5	-1040	-254.5	148	SEG44	516	219.5
15	D6	-985	-254.5	149	SEG45	492	89.5
16	GNDL	-935	-254.5	150	SEG46	468	219.5
17	D7	-885	-254.5	151	SEG47	444	89.5
18	VDD1	-830	-254.5	152	SEG48	420	219.5
19	VDD1	-775	-254.5	153	SEG49	396	89.5
20	VDD2	-720	-254.5	154	SEG50	372	219.5
21	VDD2	-665	-254.5	155	SEG51	348	89.5
22	VDD2	-610	-254.5	156	SEG52	324	219.5

23	VDD3	-555	-254.5	157	SEG53	300	89.5
24	GND1	-500	-254.5	158	SEG54	276	219.5
25	GND1	-445	-254.5	159	SEG55	252	89.5
26	GND3	-390	-254.5	160	SEG56	228	219.5
27	GND2	-335	-254.5	161	SEG57	204	89.5
28	GND2	-280	-254.5	162	SEG58	180	219.5
29	GND2	-225	-254.5	163	SEG59	156	89.5
30	V0I	-170	-254.5	164	SEG60	132	219.5
31	V0I	-115	-254.5	165	SEG61	108	89.5
32	V0I	-60	-254.5	166	SEG62	84	219.5
33	V0O	-5	-254.5	167	SEG63	60	89.5
34	V0O	50	-254.5	168	SEG64	36	219.5
35	XV0O	105	-254.5	169	SEG65	12	89.5
36	XV0O	160	-254.5	170	SEG66	-12	219.5
37	XV0I	215	-254.5	171	SEG67	-36	89.5
38	XV0I	270	-254.5	172	SEG68	-60	219.5
39	XV0I	325	-254.5	173	SEG69	-84	89.5
40	VMO	380	-254.5	174	SEG70	-108	219.5
41	VMO	435	-254.5	175	SEG71	-132	89.5
42	VGI	490	-254.5	176	SEG72	-156	219.5
43	VGI	545	-254.5	177	SEG73	-180	89.5
44	VGI	600	-254.5	178	SEG74	-204	219.5
45	VGO	655	-254.5	179	SEG75	-228	89.5
46	T6	702.5	-254.5	180	SEG76	-252	219.5
47	T7	742.5	-254.5	181	SEG77	-276	89.5
48	T8	782.5	-254.5	182	SEG78	-300	219.5
49	TFCOM	822.5	-254.5	183	SEG79	-324	89.5
50	T1	862.5	-254.5	184	SEG80	-348	219.5
51	T2	902.5	-254.5	185	SEG81	-372	89.5
52	T3	942.5	-254.5	186	SEG82	-396	219.5
53	T4	982.5	-254.5	187	SEG83	-420	89.5
54	T5	1022.5	-254.5	188	SEG84	-444	219.5
55	VREF	1065	-254.5	189	SEG85	-468	89.5
56	GNDL	1110	-254.5	190	SEG86	-492	219.5
57	VDDH	1155	-254.5	191	SEG87	-516	89.5
58	TSEL	1200	-254.5	192	SEG88	-540	219.5
59	C86	1245	-254.5	193	SEG89	-564	89.5
60	VDDH	1290	-254.5	194	SEG90	-588	219.5
61	PSB	1335	-254.5	195	SEG91	-612	89.5
62	GNDL	1380	-254.5	196	SEG92	-636	219.5
63	SI2	1425	-254.5	197	SEG93	-660	89.5
64	VDDH	1470	-254.5	198	SEG94	-684	219.5
65	SEL1	1515	-254.5	199	SEG95	-708	89.5
66	GNDL	1560	-254.5	200	SEG96	-732	219.5
67	SEL2	1605	-254.5	201	SEG97	-756	89.5

68	VDD1	1650	-254.5	202	SEG98	-780	219.5
69	VDD2	1695	-254.5	203	SEG99	-804	89.5
70	VDD3	1740	-254.5	204	SEG100	-828	219.5
71	COM62	2009.5	-257.5	205	SEG101	-852	89.5
72	COM60	2009.5	-231.5	206	SEG102	-876	219.5
73	COM58	2009.5	-205.5	207	SEG103	-900	89.5
74	COM56	2009.5	-179.5	208	SEG104	-924	219.5
75	COM54	2009.5	-153.5	209	SEG105	-948	89.5
76	COM52	2009.5	-127.5	210	SEG106	-972	219.5
77	COM50	2009.5	-101.5	211	SEG107	-996	89.5
78	COM48	2009.5	-75.5	212	SEG108	-1020	219.5
79	COM46	2009.5	-49.5	213	SEG109	-1044	89.5
80	COM44	2009.5	-23.5	214	SEG110	-1068	219.5
81	COM42	2009.5	2.5	215	SEG111	-1092	89.5
82	COM40	2009.5	28.5	216	SEG112	-1116	219.5
83	COM38	2009.5	54.5	217	SEG113	-1140	89.5
84	COM36	2009.5	80.5	218	SEG114	-1164	219.5
85	COM34	2009.5	106.5	219	SEG115	-1188	89.5
86	COM32	2009.5	132.5	220	SEG116	-1212	219.5
87	COM30	2009.5	158.5	221	SEG117	-1236	89.5
88	COM28	2009.5	184.5	222	SEG118	-1260	219.5
89	COM26	2009.5	210.5	223	SEG119	-1284	89.5
90	COM24	2009.5	236.5	224	SEG120	-1308	219.5
91	COM22	2009.5	262.5	225	SEG121	-1332	89.5
92	COM20	1880	219.5	226	SEG122	-1356	219.5
93	COM18	1856	89.5	227	SEG123	-1380	89.5
94	COM16	1832	219.5	228	SEG124	-1404	219.5
95	COM14	1808	89.5	229	SEG125	-1428	89.5
96	COM12	1784	219.5	230	SEG126	-1452	219.5
97	COM10	1760	89.5	231	SEG127	-1476	89.5
98	COM8	1736	219.5	232	SEG128	-1500	219.5
99	COM6	1712	89.5	233	SEG129	-1524	89.5
100	COM4	1688	219.5	234	SEG130	-1548	219.5
101	COM2	1664	89.5	235	SEG131	-1572	89.5
102	COM0	1640	219.5	236	COM1	-1616	219.5
103	COMS2	1616	89.5	237	COM3	-1640	89.5
104	SEG0	1572	219.5	238	COM5	-1664	219.5
105	SEG1	1548	89.5	239	COM7	-1688	89.5
106	SEG2	1524	219.5	240	COM9	-1712	219.5
107	SEG3	1500	89.5	241	COM11	-1736	89.5
108	SEG4	1476	219.5	242	COM13	-1760	219.5
109	SEG5	1452	89.5	243	COM15	-1784	89.5
110	SEG6	1428	219.5	244	COM17	-1808	219.5
111	SEG7	1404	89.5	245	COM19	-1832	89.5
112	SEG8	1380	219.5	246	COM21	-1856	219.5

113	SEG9	1356	89.5	247	COM23	-1880	89.5
114	SEG10	1332	219.5	248	COM25	-2009.5	262.5
115	SEG11	1308	89.5	249	COM27	-2009.5	236.5
116	SEG12	1284	219.5	250	COM29	-2009.5	210.5
117	SEG13	1260	89.5	251	COM31	-2009.5	184.5
118	SEG14	1236	219.5	252	COM33	-2009.5	158.5
119	SEG15	1212	89.5	253	COM35	-2009.5	132.5
120	SEG16	1188	219.5	254	COM37	-2009.5	106.5
121	SEG17	1164	89.5	255	COM39	-2009.5	80.5
122	SEG18	1140	219.5	256	COM41	-2009.5	54.5
123	SEG19	1116	89.5	257	COM43	-2009.5	28.5
124	SEG20	1092	219.5	258	COM45	-2009.5	2.5
125	SEG21	1068	89.5	259	COM47	-2009.5	-23.5
126	SEG22	1044	219.5	260	COM49	-2009.5	-49.5
127	SEG23	1020	89.5	261	COM51	-2009.5	-75.5
128	SEG24	996	219.5	262	COM53	-2009.5	-101.5
129	SEG25	972	89.5	263	COM55	-2009.5	-127.5
130	SEG26	948	219.5	264	COM57	-2009.5	-153.5
131	SEG27	924	89.5	265	COM59	-2009.5	-179.5
132	SEG28	900	219.5	266	COM61	-2009.5	-205.5
133	SEG29	876	89.5	267	COM63	-2009.5	-231.5
134	SEG30	852	219.5	268	COMS1	-2009.5	-257.5

Note:

[1] Unit: um.

[2] This is the default PAD Center Coordinate Table with 1/65 Duty.

[3] Tolerance: +/-0.05um.

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.